

Features

- RISC CPU
- Memories
 - Embedded with 64 MB DDR2, clock frequency up to 533 MHz
 - Three SD/MMC host controller (SMHC) interfaces: SD3.0/SDIO3.0/eMMC5.0
- Video Engine
 - H.265/H.264/MPEG-1/MPEG-2/MPEG-4/JPEG/VC1/Xvid/Sorenson Spark decoding, up to 1080p@60fps
 - JPEG/MJPEG encoding, up to 1080p@60fps
- Video and Graphics
 - Allwinner SmartColor2.0 post processing for an excellent display experience
 - Supports de-interlacer (DI) up to 1080p@60fps
 - Supports Graphic 2D (G2D) hardware accelerator including rotate, mixer, LBC decompression functions
- Video Output
 - RGB interface up to 1920 x 1080@60fps
 - Dual link LVDS interface up to 1920 x 1080@60fps
 - 4-lane MIPI DSI up to 1920 x 1200@60fps
 - CVBS OUT interface, supporting NTSC and PAL format
- Video Input
 - 8-bit digital camera interface
 - CVBS IN interface, supporting NTSC and PAL format (only for F133-B)
- Analog Audio Codec
 - 2 DACs and 3 ADCs
 - Analog audio interfaces: HPOUTL/R, MICIN3P/N, LINEINL/R, FMINL/R
- Two I2S/PCM external interfaces (I2S1, I2S2)
- Maximum 8 digital PDM microphones (DMIC)
- OWA TX and OWA RX, compliance with S/PDIF interface
- Security System
 - AES, DES, 3DES, RSA, MD5, SHA, HMAC
 - Integrated 2 Kbits OTP storage space
- External Peripherals
 - USB 2.0 DRD (USB0) and USB 2.0 HOST (USB1)
 - 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
 - Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
 - Up to 2 SPI controllers (SPI0, SPI1)
 - Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
 - CIR RX and CIR TX
 - 8 independent PWM channels (PWM0 to PWM7)
 - 1-ch GPADC
 - 4-ch TPADC
 - LEDC
- Package
 - eLQFP128, 14 mm x 14 mm x 1.4 mm

Revision History

| Revision | Date | Description |
|----------|--------------|--------------------------|
| 1.0 | May 24, 2021 | Initial release version. |



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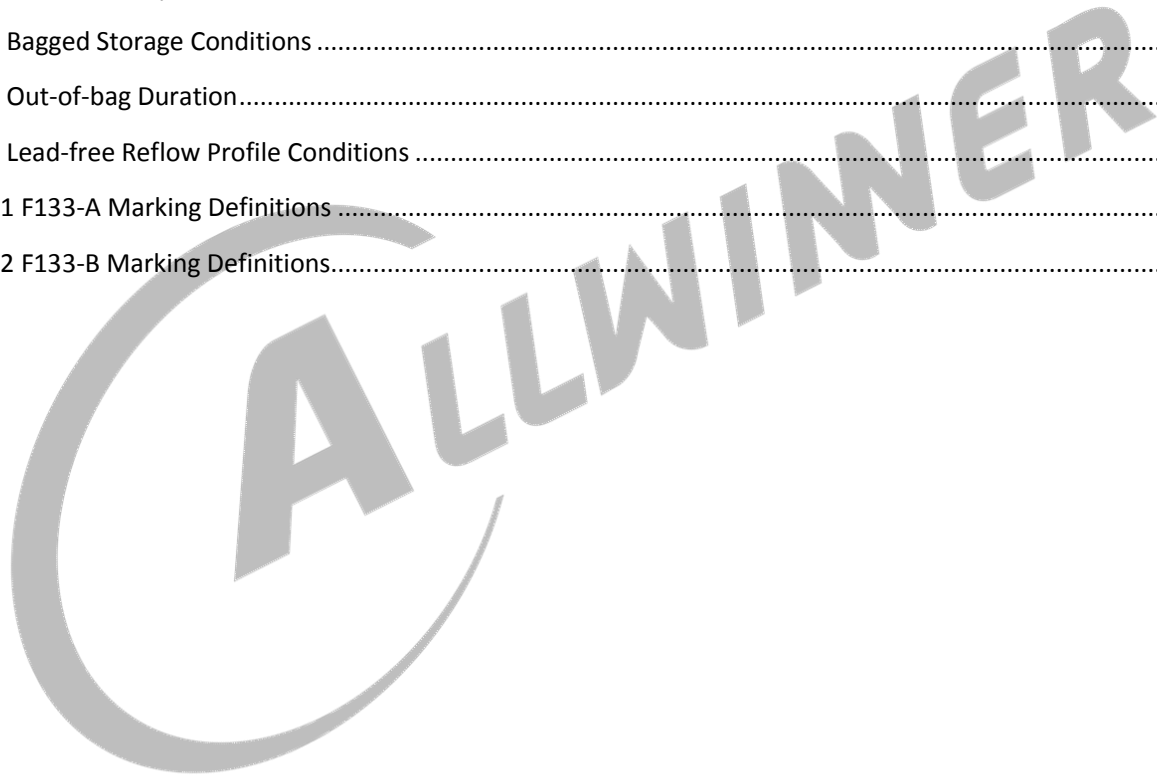
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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package, and part reliability of the F133 processor. For details about register descriptions of each module, see the [F133_User_Manual](#).

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.




| Symbol | Description |
|--|--|
|  WARNING | Indicates potential risk of injury or death exists if the instructions are not obeyed. |
|  CAUTION | Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed. |
|  NOTE | Provides additional information to emphasize or supplement important points of the main text. |

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

| Symbol | Description |
|--------|--------------------|
| - | The cell is blank. |

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

| Type | Symbol | Value |
|----------------------|--------|---------------|
| Data capacity | 1K | 1024 |
| | 1M | 1,048,576 |
| | 1G | 1,073,741,824 |
| Frequency, data rate | 1k | 1000 |
| | 1M | 1,000,000 |
| | 1G | 1,000,000,000 |



1 Overview

F133 is an advanced application processor designed for the video decoding platform. It integrates a 64-bit processor with RISC CPU instruction architecture to provide the most efficient computing power. F133 supports full format decoding such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, and so on. The independent hardware encoder can encode in JPEG or MJPEG. Integrated multi ADCs/DACs and I2S/PCM/DMIC/OWA audio interfaces can work seamlessly with the CPU to accelerate multimedia algorithms and provide the perfect voice interaction solution. F133 supports rich display output interfaces to meet the requirements of the screen display in differentiated markets. F133 can be used in network video machines, advertising machines, digital photo frames, car MP5, and so on.

1.1 Device Difference

The F133 is configured with different sets of features in different devices. Table 1-1 shows the feature differences across different devices.

Table 1-1 Device Feature Differences

| Contents | F133-A | F133-B |
|----------|------------|---------|
| CVBS IN | No support | Support |

2 Features

2.1 CPU Architecture

- RISC CPU
- 32 KB I-cache and 32 KB D-cache

2.2 Memory Subsystem

2.2.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
 - SD card
 - eMMC
 - SPI NOR Flash
 - SPI NAND Flash
- Supports mandatory upgrade process through USB and SD card
- Supports GPIO pin and eFuse module to select the boot media type

2.2.2 SDRAM

- Embedded with 64 MB DDR2
- Supports clock frequency up to 533 MHz for DDR2

2.2.3 SMHC

- Three SD/MMC host controller (SMHC) interfaces
- The SMHC0 controls the devices that comply with the protocol Secure Digital Memory (SD mem-version 3.0)
- The SMHC1 controls the device that complies with the protocol Secure Digital I/O (SDIO-version 3.0)
- The SMHC2 controls the device that complies with the protocol Multimedia Card (eMMC-version 5.0)
- Maximum performance:
 - SDR mode 150 MHz@1.8 V IO pad
 - DDR mode 50 MHz@1.8 V IO pad
 - DDR mode 50 MHz@3.3 V IO pad
- Supports 1-bit or 4-bit data width
- Supports block size of 1 to 65535 bytes

- Internal 1024-Bytes RX FIFO and 1024-Bytes TX FIFO
- Supports card insertion and removal interrupt
- Supports hardware CRC generation and error detection
- Supports descriptor-based internal DMA controller

2.3 Video Engine

- Video decoding
 - H.265 MP@L4.1 up to 1080p@60fps
 - H.264 BP/MP/HP@L4.2 up to 1080p@60fps
 - H.263 BP up to 1080p@60fps
 - MPEG-4 SP/ASP L5 up to 1080p@60fps
 - MPEG-2 MP/HL up to 1080p@60fps
 - MPEG-1 MP/HL up to 1080p@60fps
 - Xvid up to 1080p@60fps
 - Sorenson Spark up to 1080p@60fps
 - WMV9/VC-1 SP/MP/AP up to 1080p@60fps
 - MJPEG up to 1080p@30fps
- Video encoding
 - JPEG/MJPEG up to 1080p@60fps
 - Supports input picture scaler up/down

2.4 Video and Graphics

2.4.1 Display Engine (DE)

- Output size up to 2048 x 2048
- Supports two alpha blending channels for main display and one channel for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports LBC buffer decoder
- Supports dither output to TCON
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/palette
- Supports SmartColor2.0 for excellent display experience
 - Adaptive detail/edge enhancement
 - Adaptive color enhancement

- Adaptive contrast enhancement and fresh tone rectify
- Supports write back for aux display

2.4.2 De-interlacer (DI)

- Supports YUV420 (Planar/NV12/NV21) and YUV422 (Planar/NV16/NV61) data format
- Supports video resolution from 32x32 to 2048x1280 pixel
- Supports Inter-field interpolation/motion adaptive de-interlace method
- Performance: module clock 600M for 1080p@60Hz YUV420

2.4.3 Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer
- Supports horizontal flip, clockwise 0/90/270 degree rotate for LBC buffer

2.5 Video Output

2.5.1 RGB and LVDS LCD

- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports LVDS interface with dual link, up to 1920 x 1080@60fps
- Supports LVDS interface with single link, up to 1366 x 768@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL

- RGB666 and RGB565 with dither function
- Gamma correction with R/G/B channel independence

2.5.2 MIPI DSI

- Compliance with MIPI DSI v1.01
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous and non-continuous lane clock modes
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes

2.5.3 CVBS OUT

- 1-channel CVBS output
- Supports NTSC and PAL format
- Plug status auto detecting
- 10 bits DAC output

2.6 Video Input

2.6.1 Parallel CSI

- Supports 8-bit digital camera interface (RAW8/YUV422/YUV420)
- Supports BT656, BT601 interface (YUV422)
- Supports ITU-R BT.656 time-multiplexed format up to 2*1080p@30fps in DDR sample mode
- Maximum pixel clock of 148.5 MHz
- Supports de-interlacing for interlace video input
- Supports conversion from YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
- Supports horizontal and vertical flip

2.6.2 CVBS IN (Only for F133-B)

- 2-channel CVBS input and 1-channel CVBS decoder
- Supports NTSC and PAL format
- Supports YUV422/YUV420 format
- With 1 channel 3D comb filter

- Detection for signal locked and 625 lines
- Programmable brightness, contrast, and saturation
- 10-bit video ADCs

2.7 System Peripherals

2.7.1 Timer

- The timer module implements the timing and counting functions, which includes timer0, timer1, watchdog, and audio video synchronization (AVS)
- The timer0/timer1 is a 32-bit down counter. The timer0 and timer1 are completely consistent
- The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
- The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent

2.7.2 High Speed Timer (HSTimer)

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.
- Configurable 56-bit down timer
- Supports 5 prescale factors
- The clock source is synchronized with AHB0 clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.7.3 Platform-Level Interrupt Controller (PLIC)

- Sampling, priority arbitration and distribution for external interrupt sources
- The interrupt can be configured as machine mode and super user mode
- Up to 256 interrupt source sampling, supporting level interrupt and pulse interrupt
- 32 levels of interrupt priority
- Maintains independently the interrupt enable for each interrupt mode (machine/super user)
- Maintains independently the interrupt threshold for each interrupt mode (machine/super user)
- Configurable access permission for PLIC registers

2.7.4 DMAC

- Up to 16-ch DMA
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing

- Flexible data width of 8/16/32/64-bit
- Programmable DMA burst length
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transferring data with a linked list
- DRQ response includes waiting mode and handshake mode
- DMA channel supports pause function
- Memory devices support non-aligned transform

2.7.5 Clock Controller Unit (CCU)

- 8 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.7.6 Thermal Sensor Controller (THS)

- One thermal sensor located in CPU
- Temperature accuracy: $\pm 3^{\circ}\text{C}$ from 0°C to $+100^{\circ}\text{C}$, $\pm 5^{\circ}\text{C}$ from -25°C to $+125^{\circ}\text{C}$
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.7.7 LDO Power

- Integrated 2 LDOs (LDOA, LDOB)
- LDOA: 1.8 V power output, LDOB: 1.35 V/1.5 V/1.8 V power output
- LDOA for IO and analog module, LDOB for SDRAM
- Input voltage is 2.4 V to 3.6 V

2.7.8 RTC

- Implements time counter and timing wakeup
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock

- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information

2.7.9 I/O Memory Management Unit (IOMMU)

- Supports virtual address to physical address mapping by hardware implementation
- Supports VE, CSI, DE, G2D, DI parallel address mapping
- Supports VE, CSI, DE, G2D, DI bypass function independently
- Supports VE, CSI, DE, G2D, DI pre-fetch independently
- Supports VE, CSI, DE, G2D, DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.8 Audio Subsystem

2.8.1 Audio Codec

- Two audio digital-to-analog converter (DAC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 192 kHz DAC sample rate
 - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- One audio output:
 - One stereo headphone output: HPOUTL/R
- Three audio analog-to-digital converter (ADC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 48 kHz ADC sample rate
 - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD+N
- Three audio inputs:
 - One differential microphone input: MICIN3P/3N, or one single-end microphone input: MICIN3P
 - One stereo LINEIN input: LINEINL/R
 - One stereo FMIN input: FMINL/R
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive

- Programmable FIFO thresholds
- Supports interrupts and DMA
- Internal HPLDO output for HPVCC
- Internal ALDO output for AVCC

2.8.2 I2S/PCM

- Two I2S/PCM external interfaces (I2S1, I2S2) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
 - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
 - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
 - Programmable FIFO thresholds
 - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
 - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
 - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
 - Up to 16 channels ($f_s = 48$ kHz) which has adjustable width from 8-bit to 32-bit
 - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
 - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

2.8.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.8.4 One Wire Audio (OWA)

- One OWA TX and one OWA RX
- Compliance with S/PDIF interface
- IEC-60958 and IEC-61937 transmitter and receiver functionality
 - IEC-60958 supports 16-bit, 20-bit, and 24-bit data formats

- IEC-61937 uses the IEC-60958 series for the conveying of non-linear PCM bit streams, each sub-frame transmits 16-bit
- TXFIFO and RXFIFO
 - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
 - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Supports multiple function clock
 - Separate clock for OWA TX and OWA RX
 - The clock of TX function includes 24.576 MHz and 22.579 MHz frequency
 - The clock of RX function includes 24.576*8MHz frequency
- Supports hardware parity on TX/RX
 - Hardware parity checking on the receiver
 - Hardware parity generation on the transmitter
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter
- Supports interrupts and DMA

2.9 Security System

2.9.1 Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, TDES
 - Supports ECB, CBC, CTS, CTR, CFB, OFB mode for AES
 - Supports 128/192/256-bit key for AES
 - Supports ECB, CBC, CTR mode for DES/TDES
- Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC
 - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
 - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
 - Supports multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Supports Asymmetrical algorithm for signature verification: RSA
 - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal DMA controller for data transfer with memory

2.9.2 Security ID (SID)

- Supports 2 Kbits eFuse
- Backup eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key use status in the SID
- Loading the key to the CE

2.10 External Peripherals

2.10.1 USB DRD

- One USB 2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB Host function
 - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
 - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
 - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
 - Supports only 1 USB Root port shared between EHCI and OHCI
- Supports USB Device function
 - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
 - Supports bi-directional endpoint0 (EP0) for Control transfer
 - Up to 10 user-configurable endpoints (EP1+, EP1-, EP2+, EP2-, EP3+, EP3-, EP4+, EP4-, EP5+, EP5-) for Bulk transfer, Isochronous transfer and Interrupt transfer
 - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
 - Support interface to an external Normal DMA controller for every EP
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Device and host controller share a 8K SRAM and a physical PHY

2.10.2 USB HOST

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB2.0 Host function
 - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
 - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
 - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
 - Supports only 1 USB Root port shared between EHCI and OHCI
- An internal DMA Controller for data transfer with memory

2.10.3 EMAC

- One EMAC interface for connecting external Ethernet PHY
- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operations
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
 - Supports linked-list descriptor list structure
 - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
 - Comprehensive status reporting for normal operation and transfers with errors
- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.10.4 UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
- UART0, UART4, UART5: 2-wire; UART1, UART2, UART3: 4-wire
- Compatible with industry-standard 16450/16550 UARTs
- Supports IrDA-compatible slow infrared (SIR) format
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO

- Each of them is 64 bytes (For UART0)
- Each of them is 256 bytes (For UART1, UART2, UART3, UART4, and UART5)
- The working reference clock is from the APB bus clock
 - Speed up to 4 Mbit/s with 64 MHz APB clock
 - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 characters, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports RX DMA Master interface (Only for UART1)
- Supports auto-flow by using CTS & RTS (Only for UART1/2/3)

2.10.5 SPI and SPI_DBI

- Up to 2 SPI controllers (SPI0, SPI1)
- The SPI0 only supports SPI mode; The SPI1 supports SPI mode and display bus interface (DBI) mode
- SPI mode:
 - Full-duplex synchronous serial interface
 - Master/slave configurable
 - Mode0 to Mode3 are supported for both transmit and receive operations
 - 8-bit wide by 64-entry FIFO for both transmit and receive data
 - Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
 - Supports 3-wire/4-wire SPI
 - Supports programmable serial data frame length: 1-bit to 32-bit
 - Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI
- DBI mode:
 - Supports DBI Type C 3 Line/4 Line Interface Mode
 - Supports 2 Data Lane Interface Mode
 - Supports RGB111/444/565/666/888 video format
 - Maximum resolution of RGB666 240 x 320@30Hz with single data lane
 - Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
 - Supports Tearing effect
 - Supports software flexible control video frame rate

2.10.6 Two Wire Interface (TWI)

- Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
- Compliant with I2C bus standard
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s)
- Supports 7-bit and 10-bit device addressing modes
- Supports master mode or slave mode
- Master mode features:
 - Supports the bus arbitration in the case of multiple master devices
 - Supports clock synchronization and bit and byte waiting
 - Supports packet transmission and DMA
- Slave mode features:
 - Interrupt on address detection
- The TWI controller includes one TWI engine and one TWI driver. And the TWI driver supports packet transmission and DMA mode when TWI works in master mode

2.10.7 CIR Receiver (CIR_RX)

- One CIR_RX interface (IR-RX)
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.10.8 CIR Transmitter (CIR_TX)

- One CIR_TX interface (IR-TX)
- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer

2.10.9 PWM

- Supports 8 independent PWM channels (PWM0 to PWM7)
 - Supports PWM continuous mode output
 - Supports PWM pulse mode output, and the pulse number is configurable

- Output frequency range: 0 to 24 MHz or 100 MHz
- Various duty-cycle: 0% to 100%
- Minimum resolution: 1/65536
- Supports 4 complementary pairs output
 - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7)
 - Supports dead-zone generator, and the dead-zone time is configurable
- Supports 4 group of PWM channel output for controlling stepping motors
 - Supports any plural channels to form a group, and output the same duty-cycle pulse
 - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports 8 channels capture input
 - Supports rising edge detection and falling edge detection for input waveform pulse
 - Supports pulse-width measurement for input waveform pulse

2.10.10 General Purpose ADC (GPADC)

- 1-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 12-bit sampling resolution and 8-bit precision
- 64 FIFO depth of data register
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

2.10.11 Touch Panel ADC (TPADC)

- 12 bit SAR type A/D converter
- Configurable sample frequency up to 1 MHz
- One 32x12 FIFO for storing A/D conversion result
- Supports DMA slave interface
- Supports 4-wire resistive touch panel input detection
 - Supports pen down detection with programmable sensitivity
 - Supports single touch coordinate measurement
 - Supports dual touch detection
 - Supports touch pressure measurement with programmable threshold
 - Supports median and averaging filter for noise reduction
 - Supports X and Y coordinate exchange function

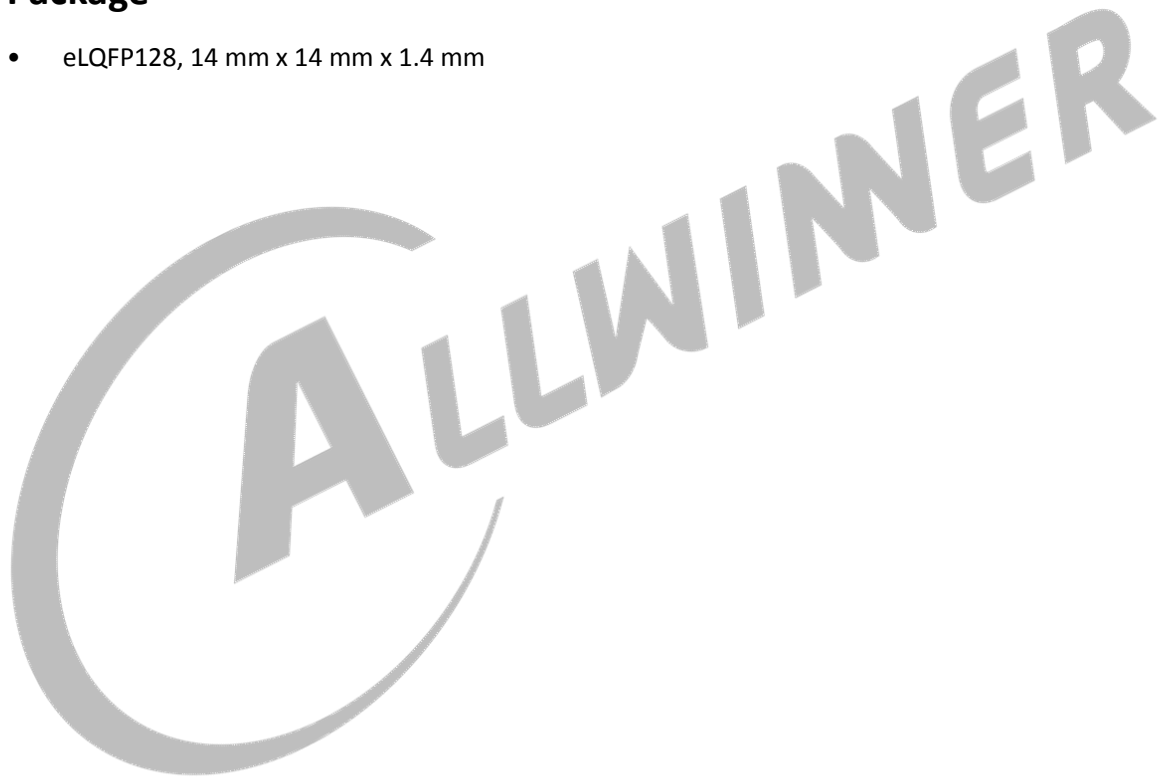
- Supports Aux ADC with up to 4 channels

2.10.12 LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s

2.11 Package

- eLQFP128, 14 mm x 14 mm x 1.4 mm



3 Block Diagram

Figure 3-1 shows the system block diagram of the F133.

Figure 3-1 F133 System Block Diagram

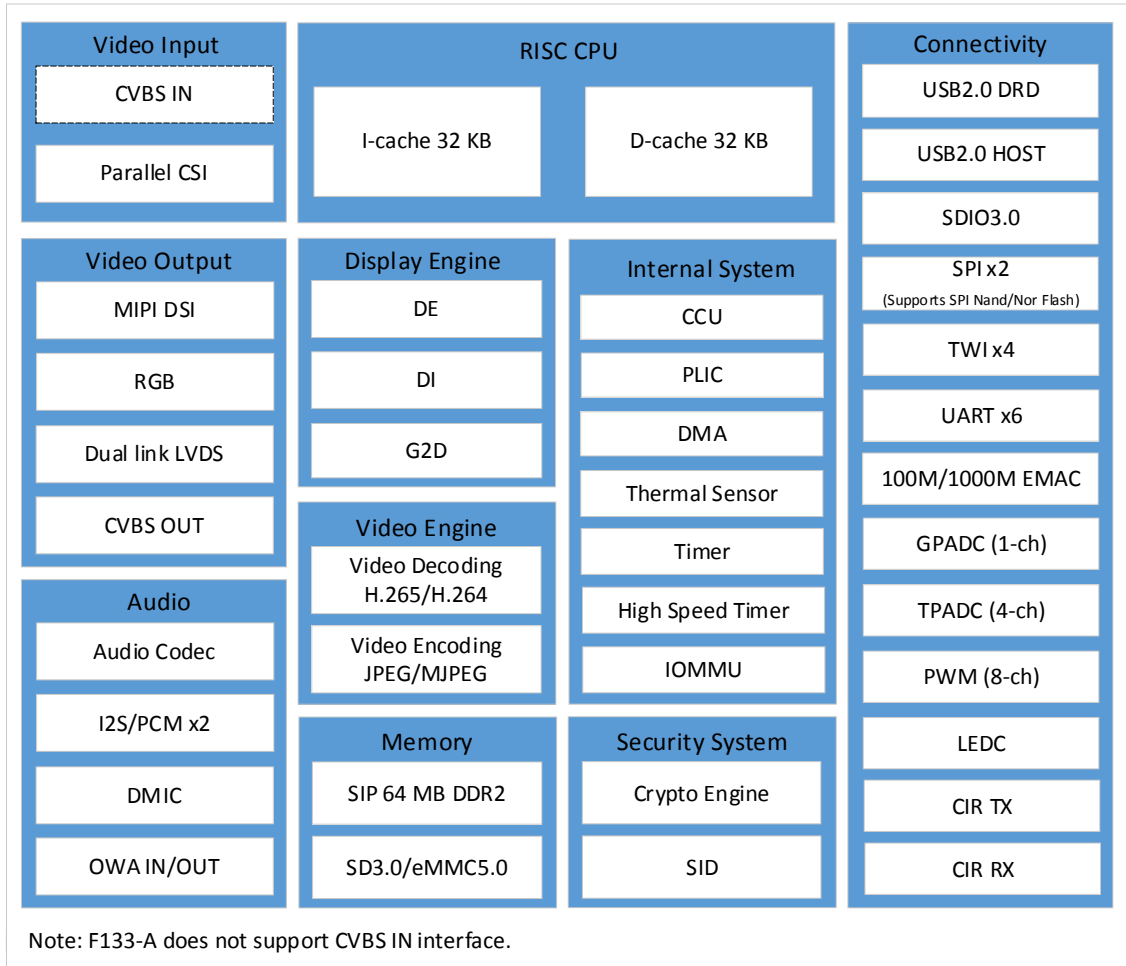
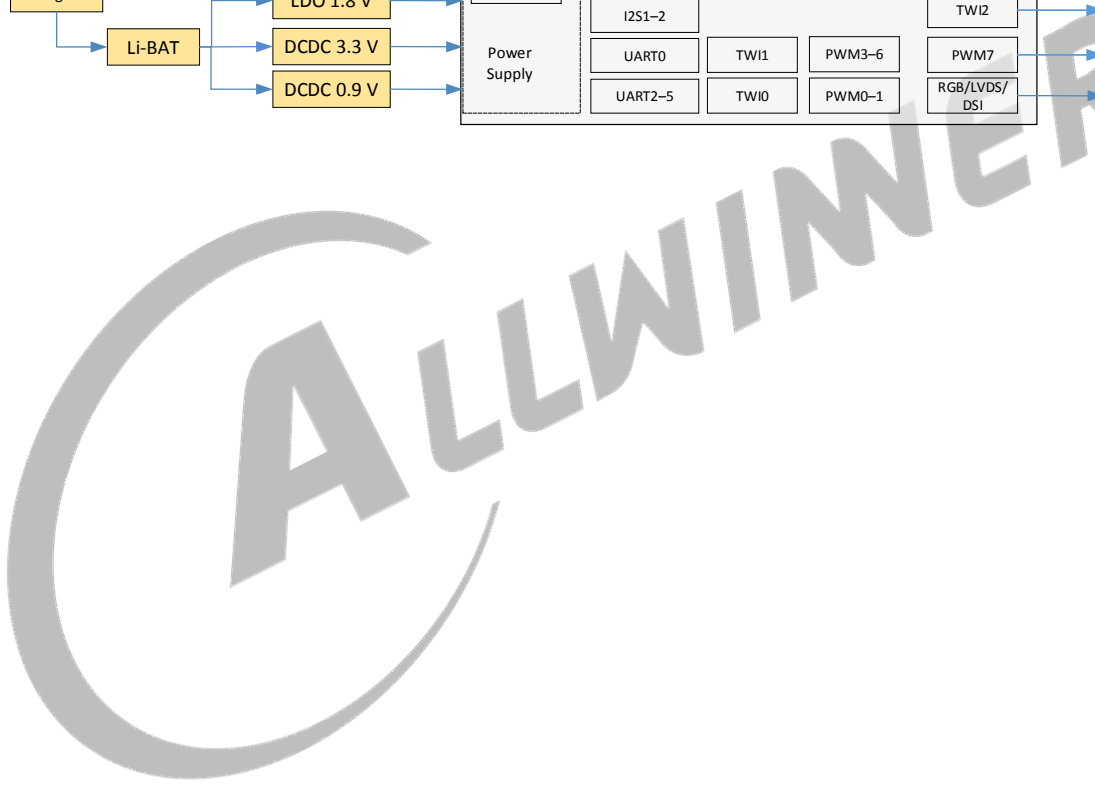
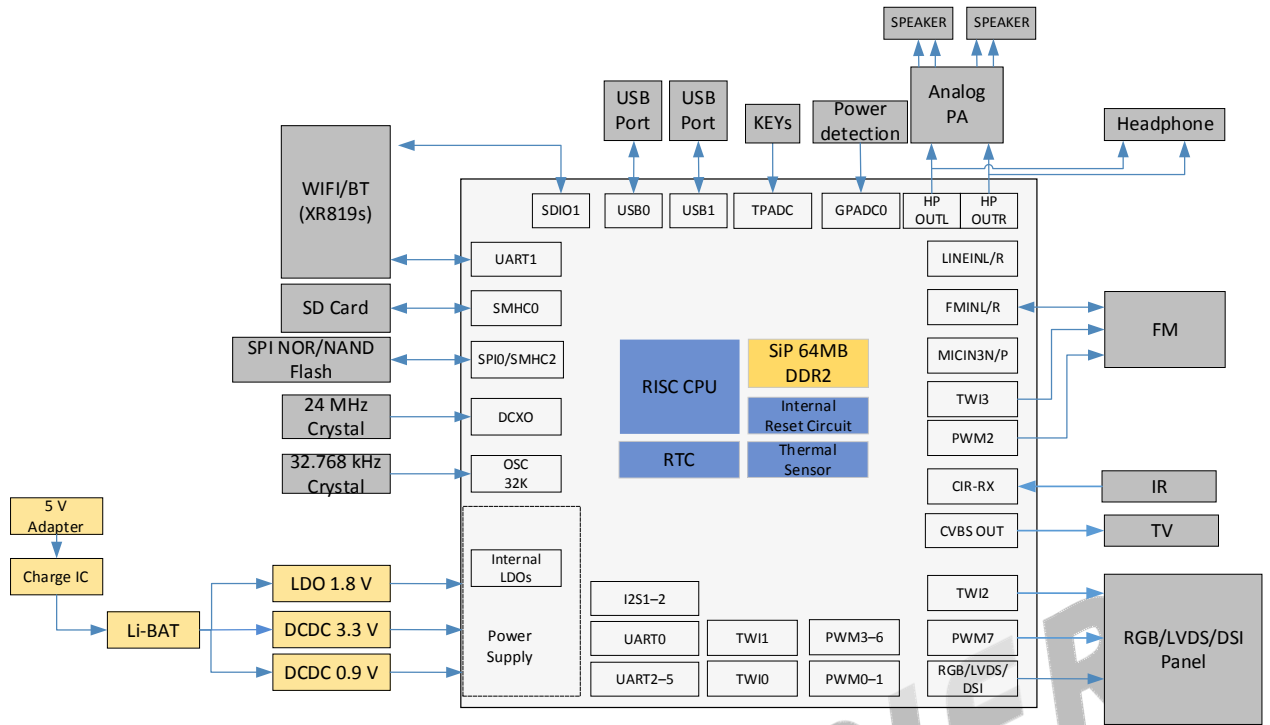


Figure 3-2 shows the intelligent speaker solution of the F133.

Figure 3-2 F133 Intelligent Speaker Solution



4 Pin Description

4.1 Pin Quantity

Table 4-1 lists the pin quantity of the F133.

Table 4-1 F133 Pin Quantity

| Pin Type | F133-A Quantity | F133-B Quantity |
|-----------|-----------------|-----------------|
| I/O | 99 | 101 |
| NC | 7 | 2 |
| Power | 18 | 21 |
| Ground | 1 | 1 |
| DDR Power | 3 | 3 |
| Total | 128 | 128 |

4.2 Pin Characteristics

Table 4-2 lists the characteristics of the F133 pins from the following seven aspects.

[1].**Ball#**: Package ball numbers associated with each signal.

[2].**Pin Name**: The name of the package pin.

[3].**Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4].**Ball Reset State**: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].**Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

[6].**Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

[7].**Power Supply**: The voltage supply for the IO buffers of the terminal.

Table 4-2 Pin Characteristics

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|----------------------|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| SDRAM | | | | | | | | |
| 48 | VCC-DRAM0 | P | NA | | NA | NA | | NA |
| 49 | VCC-DRAM1 | P | NA | | NA | NA | | NA |
| 50 | VDD18-DRAM | P | NA | | NA | NA | | NA |
| GPIOB | | | | | | | | |
| 86 | PB2 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 85 | PB3 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 84 | PB4 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 82 | PB5 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 80 | PB6 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 79 | PB7 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| GPIOC | | | | | | | | |
| 19 | PC2 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 18 | PC3 | I/O | PU | | PU/PD | 4 | | VCC-IO |
| 17 | PC4 | I/O | PU | | PU/PD | 4 | | VCC-IO |
| 16 | PC5 | I/O | PU | | PU/PD | 4 | | VCC-IO |
| 15 | PC6 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 14 | PC7 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| GPIOD | | | | | | | | |
| 55 | PD0 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 56 | PD1 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 57 | PD2 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 58 | PD3 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 59 | PD4 | I/O | Z | | PU/PD | 4 | | VCC-PD |

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|----------------------|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| 60 | PD5 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 61 | PD6 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 62 | PD7 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 63 | PD8 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 64 | PD9 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 67 | PD10 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 68 | PD11 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 70 | PD12 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 69 | PD13 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 71 | PD14 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 72 | PD15 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 73 | PD16 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 74 | PD17 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 75 | PD18 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 76 | PD19 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 54 | PD20 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 53 | PD21 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 52 | PD22 | I/O | Z | | PU/PD | 4 | | VCC-PD |
| 65 | VCC-LVDS | P | NA | | NA | NA | | NA |
| 66 | VCC-PD | P | NA | | NA | NA | | NA |
| GPIOE | | | | | | | | |
| 44 | PE0 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 45 | PE1 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 35 | PE2 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 33 | PE3 | I/O | Z | | PU/PD | 4 | | VCC-PE |

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|----------------------|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| 43 | PE4 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 42 | PE5 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 41 | PE6 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 40 | PE7 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 39 | PE8 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 38 | PE9 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 37 | PE10 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 36 | PE11 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 32 | PE12 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 31 | PE13 | I/O | Z | | PU/PD | 4 | | VCC-PE |
| 34 | VCC-PE | P | NA | | NA | NA | | NA |
| GPIOF | | | | | | | | |
| 7 | PF0 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 8 | PF1 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 9 | PF2 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 10 | PF3 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 11 | PF4 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 12 | PF5 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| 13 | PF6 | I/O | Z | | PU/PD | 4 | | VCC-IO |
| GPIOG | | | | | | | | |
| 120 | PG0 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 118 | PG1 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 119 | PG2 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 121 | PG3 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 123 | PG4 | I/O | Z | | PU/PD | 4 | | VCC-PG |

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|----------------------|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| 122 | PG5 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 1 | PG6 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 2 | PG7 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 3 | PG8 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 4 | PG9 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 5 | PG10 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 6 | PG11 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 124 | PG12 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 125 | PG13 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 126 | PG14 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 127 | PG15 | I/O | Z | | PU/PD | 4 | | VCC-PG |
| 128 | VCC-PG | P | NA | | NA | NA | | NA |
| System | | | | | | | | |
| 27 | RESET | I, OD | NA | | NA | NA | | VCC-RTC |
| GPADC | | | | | | | | |
| 101 | GPADC0 | AI | NA | | NA | NA | | AVCC |
| TPADC | | | | | | | | |
| 102 | TP-X1 | AI | NA | | NA | NA | | AVCC |
| 103 | TP-X2 | AI | NA | | NA | NA | | AVCC |
| 104 | TP-Y1 | AI | NA | | NA | NA | | AVCC |
| 105 | TP-Y2 | AI | NA | | NA | NA | | AVCC |
| USB | | | | | | | | |
| 114 | USB0-DM | A I/O | NA | | NA | NA | | VCC-IO |
| 115 | USB0-DP | A I/O | NA | | NA | NA | | VCC-IO |
| 113 | USB1-DM | A I/O | NA | | NA | NA | | VCC-IO |

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|---|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| 112 | USB1-DP | A I/O | NA | | NA | NA | | VCC-IO |
| CVBS OUT | | | | | | | | |
| 78 | TVOUT0 | AO | NA | | NA | NA | | VCC-TVOUT |
| 77 | VCC-TVOUT | P | NA | | NA | NA | | NA |
| CVBS IN (Only for F133-B) ⁽¹⁾ | | | | | | | | |
| 108 | TVIN0 | AI | NA | | NA | NA | | VCC-TVIN |
| 109 | TVIN1 | AI | NA | | NA | NA | | VCC-TVIN |
| 110 | TVIN-VRP | P | NA | | NA | NA | | VCC-TVIN |
| 111 | TVIN-VRN | P | NA | | NA | NA | | VCC-TVIN |
| 107 | VCC-TVIN | P | NA | | NA | NA | | NA |
| Audio Codec | | | | | | | | |
| 87 | MICIN3P | AI | NA | | NA | NA | | AVCC |
| 88 | MICIN3N | AI | NA | | NA | NA | | AVCC |
| 93 | FMINR | AI | NA | | NA | NA | | AVCC |
| 94 | FMINL | AI | NA | | NA | NA | | AVCC |
| 95 | LINEINR | AI | NA | | NA | NA | | AVCC |
| 96 | LINEINL | AI | NA | | NA | NA | | AVCC |
| 98 | HPOUTR | AO | NA | | NA | NA | | HPVCC |
| 99 | HPOUTL | AO | NA | | NA | NA | | HPVCC |
| 100 | HPOUTFB | AI | NA | | NA | NA | | HPVCC |
| 97 | HPVCC | P | NA | | NA | NA | | NA |
| 92 | VRA1 | AO | NA | | NA | NA | | AVCC |
| 90 | VRA2 | AO | NA | | NA | NA | | AVCC |
| 89 | AVCC | P | NA | | NA | NA | | NA |
| 91 | AGND | G | NA | | NA | NA | | NA |

| Ball# ^[1] | Pin Name ^[2] | Type ^[3] | Ball State ^[4] | Reset | Pull Up/Down ^[5] | Default Strength ^[6] (mA) | Buffer | Power Supply ^[7] |
|----------------------|-------------------------|---------------------|---------------------------|-------|-----------------------------|--------------------------------------|--------|-----------------------------|
| RTC & PLL | | | | | | | | |
| 25 | X32KIN | AI | NA | | NA | NA | | VCC-RTC |
| 24 | X32KOUT | AO | NA | | NA | NA | | VCC-RTC |
| 26 | VCC-RTC | P | NA | | NA | NA | | NA |
| 20 | VCC-PLL | P | NA | | NA | NA | | NA |
| DCXO | | | | | | | | |
| 23 | DXIN | AI | NA | | NA | NA | | VCC-PLL |
| 22 | DXOUT | AO | NA | | NA | NA | | VCC-PLL |
| 21 | REFCLK-OUT | AO | NA | | NA | NA | | VCC-PLL |
| NC | | | | | | | | |
| 47 | NC | NA | NA | | NA | NA | | NA |
| 106 | NC0 | NA | NA | | NA | NA | | NA |
| Power | | | | | | | | |
| 29 | LDO-IN | P | NA | | NA | NA | | NA |
| 28 | LDOA-OUT | P | NA | | NA | NA | | NA |
| 30 | LDOB-OUT | P | NA | | NA | NA | | NA |
| 83 | VCC-IO | P | NA | | NA | NA | | NA |
| 46 | VDD-SYS0 | P | NA | | NA | NA | | NA |
| 51 | VDD-SYS1 | P | NA | | NA | NA | | NA |
| 81 | VDD-SYS2 | P | NA | | NA | NA | | NA |
| 116 | VDD-CORE0 | P | NA | | NA | NA | | NA |
| 117 | VDD-CORE1 | P | NA | | NA | NA | | NA |

(1) For F133-A, these pins (107, 108, 109, 110, 111) are NC.

4.3 GPIO Multiplex Function

The following table provides a description of the F133 GPIO multiplex function.



NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

Table 4-3 GPIO Multiplex Function

| Pin Name | GPIO Group | IO Type | Function2 | Function3 | Function4 | Function5 | Function6 | Function7 | Function8 | Function14 |
|----------|------------|----------|-----------|------------|--------------------------------------|-----------|-----------|-----------|-----------|------------|
| PB2 | GPIOB | I/O | LCD0-D0 | I2S2-DOUT2 | TWI0-SDA | I2S2-DIN2 | LCD0-D18 | UART4-TX | | PB-EINT2 |
| PB3 | | I/O | LCD0-D1 | I2S2-DOUT1 | TWI0-SCK | I2S2-DIN0 | LCD0-D19 | UART4-RX | | PB-EINT3 |
| PB4 | | I/O | LCD0-D8 | I2S2-DOUT0 | TWI1-SCK | I2S2-DIN1 | LCD0-D20 | UART5-TX | | PB-EINT4 |
| PB5 | | I/O | LCD0-D9 | I2S2-BCLK | TWI1-SDA | PWM0 | LCD0-D21 | UART5-RX | | PB-EINT5 |
| PB6 | | I/O | LCD0-D16 | I2S2-LRCK | TWI3-SCK | PWM1 | LCD0-D22 | UART3-TX | CPUBIST0 | PB-EINT6 |
| PB7 | | I/O | LCD0-D17 | I2S2-MCLK | TWI3-SDA | IR-RX | LCD0-D23 | UART3-RX | CPUBIST1 | PB-EINT7 |
| PC2 | GPIOC | I/O | SPI0-CLK | SDC2-CLK | | | | | | PC-EINT2 |
| PC3 | | I/O | SPI0-CS0 | SDC2-CMD | | | | | | PC-EINT3 |
| PC4 | | I/O | SPI0-MOSI | SDC2-D2 | BOOT-SEL0 | | | | | PC-EINT4 |
| PC5 | | I/O | SPI0-MISO | SDC2-D1 | BOOT-SEL1 | | | | | PC-EINT5 |
| PC6 | | I/O | SPI0-WP | SDC2-D0 | UART3-TX | TWI3-SCK | DBG-CLK | | | PC-EINT6 |
| PC7 | | I/O | SPI0-HOLD | SDC2-D3 | UART3-RX | TWI3-SDA | TCON-TRIG | | | PC-EINT7 |
| PD0 | GPIOD | I/O | LCD0-D2 | LVDS0-V0P | DSI-D0P | TWI0-SCK | | | | PD-EINT0 |
| PD1 | | I/O | LCD0-D3 | LVDS0-V0N | DSI-D0N | UART2-TX | | | | PD-EINT1 |
| PD2 | | I/O | LCD0-D4 | LVDS0-V1P | DSI-D1P | UART2-RX | | | | PD-EINT2 |
| PD3 | | I/O | LCD0-D5 | LVDS0-V1N | DSI-D1N | UART2-RTS | | | | PD-EINT3 |
| PD4 | | I/O | LCD0-D6 | LVDS0-V2P | DSI-CKP | UART2-CTS | | | | PD-EINT4 |
| PD5 | | I/O | LCD0-D7 | LVDS0-V2N | DSI-CKN | UART5-TX | | | | PD-EINT5 |
| PD6 | | I/O | LCD0-D10 | LVDS0-CKP | DSI-D2P | UART5-RX | | | | PD-EINT6 |
| PD7 | | I/O | LCD0-D11 | LVDS0-CKN | DSI-D2N | UART4-TX | | | | PD-EINT7 |
| PD8 | | I/O | LCD0-D12 | LVDS0-V3P | DSI-D3P | UART4-RX | | | | PD-EINT8 |
| PD9 | | I/O | LCD0-D13 | LVDS0-V3N | DSI-D3N | PWM6 | | | | PD-EINT9 |
| PD10 | | I/O | LCD0-D14 | LVDS1-V0P | SPI1-CS/DBI-CSX | UART3-TX | | | | PD-EINT10 |
| PD11 | | I/O | LCD0-D15 | LVDS1-V0N | SPI1-CLK/DBI-SCLK | UART3-RX | | | | PD-EINT11 |
| PD12 | | I/O | LCD0-D18 | LVDS1-V1P | SPI1-MOSI/DBI-SDO | TWI0-SDA | | | | PD-EINT12 |
| PD13 | | I/O | LCD0-D19 | LVDS1-V1N | SPI1-MISO/DBI-SDI/ DBI-TE/DBI-DCX | UART3-RTS | | | | PD-EINT13 |
| PD14 | | I/O | LCD0-D20 | LVDS1-V2P | SPI1-HOLD/DBI-DCX /DBI-WRX | UART3-CTS | | | | PD-EINT14 |
| PD15 | | I/O | LCD0-D21 | LVDS1-V2N | SPI1-WP/DBI-TE | IR-RX | | | | PD-EINT15 |
| PD16 | | I/O | LCD0-D22 | LVDS1-CKP | DMIC-DATA3 | PWM0 | | | | PD-EINT16 |
| PD17 | I/O | LCD0-D23 | LVDS1-CKN | DMIC-DATA2 | PWM1 | | | | PD-EINT17 | |

| Pin Name | GPIO Group | IO Type | Function2 | Function3 | Function4 | Function5 | Function6 | Function7 | Function8 | Function14 |
|----------|------------|----------|-------------|-------------|---------------------------|-------------|-----------|------------|---------------------------|------------|
| PD18 | | I/O | LCD0-CLK | LVDS1-V3P | DMIC-DATA1 | PWM2 | | | | PD-EINT18 |
| PD19 | | I/O | LCD0-DE | LVDS1-V3N | DMIC-DATA0 | PWM3 | | | | PD-EINT19 |
| PD20 | | I/O | LCD0-HSYNC | TWI2-SCK | DMIC-CLK | PWM4 | | | | PD-EINT20 |
| PD21 | | I/O | LCD0-VSYNC | TWI2-SDA | UART1-TX | PWM5 | | | | PD-EINT21 |
| PD22 | | I/O | OWA-OUT | IR-RX | UART1-RX | PWM7 | | | | PD-EINT22 |
| PE0 | GPIOE | I/O | NCSI0-HSYNC | UART2-RTS | TWI1-SCK | LCD0-HSYNC | | | RGMII-RXCTRL /RMII-CRS-DV | PE-EINT0 |
| PE1 | | I/O | NCSI0-VSYNC | UART2-CTS | TWI1-SDA | LCD0-VSYNC | | | RGMII-RXD0/ RMII-RXD0 | PE-EINT1 |
| PE2 | | I/O | NCSI0-PCLK | UART2-TX | TWI0-SCK | CLK-FANOUT0 | UART0-TX | | RGMII-RXD1/ RMII-RXD1 | PE-EINT2 |
| PE3 | | I/O | NCSI0-MCLK | UART2-RX | TWI0-SDA | CLK-FANOUT1 | UART0-RX | | RGMII-TXCK/ RMII-TXCK | PE-EINT3 |
| PE4 | | I/O | NCSI0-D0 | UART4-TX | TWI2-SCK | CLK-FANOUT2 | | R-JTAG-MS | RGMII-TXD0/ RMII-TXD0 | PE-EINT4 |
| PE5 | | I/O | NCSI0-D1 | UART4-RX | TWI2-SDA | LEDC-DO | | R-JTAG-DI | RGMII-TXD1/ RMII-TXD1 | PE-EINT5 |
| PE6 | | I/O | NCSI0-D2 | UART5-TX | TWI3-SCK | OWA-IN | | R-JTAG-DO | RGMII-TXCTRL /RMII-TXEN | PE-EINT6 |
| PE7 | | I/O | NCSI0-D3 | UART5-RX | TWI3-SDA | OWA-OUT | | R-JTAG-CK | RGMII-CLKIN/ RMII-RXER | PE-EINT7 |
| PE8 | | I/O | NCSI0-D4 | UART1-RTS | PWM2 | UART3-TX | | | MDC | PE-EINT8 |
| PE9 | | I/O | NCSI0-D5 | UART1-CTS | PWM3 | UART3-RX | | | MDIO | PE-EINT9 |
| PE10 | | I/O | NCSI0-D6 | UART1-TX | PWM4 | IR-RX | | | EPHY-25M | PE-EINT10 |
| PE11 | | I/O | NCSI0-D7 | UART1-RX | | | | | RGMII-TXD2 | PE-EINT11 |
| PE12 | | I/O | TWI2-SCK | NCSI0-FIELD | | | | | RGMII-TXD3 | PE-EINT12 |
| PE13 | I/O | TWI2-SDA | PWM5 | | | DMIC-DATA3 | | RGMII-RXD2 | PE-EINT13 | |
| PF0 | GPIOF | I/O | SDC0-D1 | | R-JTAG-MS | I2S2-DOUT1 | I2S2-DIN0 | | | PF-EINT0 |
| PF1 | | I/O | SDC0-D0 | | R-JTAG-DI | I2S2-DOUT0 | I2S2-DIN1 | | | PF-EINT1 |
| PF2 | | I/O | SDC0-CLK | UART0-TX | TWI0-SCK | LEDC-DO | OWA-IN | | | PF-EINT2 |
| PF3 | | I/O | SDC0-CMD | | R-JTAG-DO | I2S2-BCLK | | | | PF-EINT3 |
| PF4 | | I/O | SDC0-D3 | UART0-RX | TWI0-SDA | PWM6 | IR-TX | | | PF-EINT4 |
| PF5 | | I/O | SDC0-D2 | | R-JTAG-CK | I2S2-LRCK | | | | PF-EINT5 |
| PF6 | I/O | | OWA-OUT | IR-RX | I2S2-MCLK | PWM5 | | | PF-EINT6 | |
| PG0 | GPIOG | I/O | SDC1-CLK | UART3-TX | RGMII-RXCTRL/ RMII-CRS-DV | PWM7 | | | | PG-EINT0 |
| PG1 | | I/O | SDC1-CMD | UART3-RX | RGMII-RXD0/ RMII-RXD0 | PWM6 | | | | PG-EINT1 |
| PG2 | | I/O | SDC1-D0 | UART3-RTS | RGMII-RXD1/ RMII-RXD1 | UART4-TX | | | | PG-EINT2 |
| PG3 | | I/O | SDC1-D1 | UART3-CTS | RGMII-TXCK/ RMII-TXCK | UART4-RX | | | | PG-EINT3 |
| PG4 | | I/O | SDC1-D2 | UART5-TX | RGMII-TXD0/ | PWM5 | | | | PG-EINT4 |

| Pin Name | GPIO Group | IO Type | Function2 | Function3 | Function4 | Function5 | Function6 | Function7 | Function8 | Function14 |
|----------|------------|---------|------------|-----------|----------------------------|-------------|-----------|-----------|-----------|------------|
| | | | | | RMII-TXD0 | | | | | |
| PG5 | | I/O | SDC1-D3 | UART5-RX | RGMII-TXD1/ RMII-TXD1 | PWM4 | | | | PG-EINT5 |
| PG6 | | I/O | UART1-TX | TWI2-SCK | RGMII-TXD2 | PWM1 | | | | PG-EINT6 |
| PG7 | | I/O | UART1-RX | TWI2-SDA | RGMII-TXD3 | OWA-IN | | | | PG-EINT7 |
| PG8 | | I/O | UART1-RTS | TWI1-SCK | RGMII-RXD2 | UART3-TX | | | | PG-EINT8 |
| PG9 | | I/O | UART1-CTS | TWI1-SDA | RGMII-RXD3 | UART3-RX | | | | PG-EINT9 |
| PG10 | | I/O | PWM3 | TWI3-SCK | RGMII-RXCK | CLK-FANOUT0 | IR-RX | | | PG-EINT10 |
| PG11 | | I/O | I2S1-MCLK | TWI3-SDA | EPHY-25M | CLK-FANOUT1 | TCON-TRIG | | | PG-EINT11 |
| PG12 | | I/O | I2S1-LRCK | TWI0-SCK | RGMII-TXCTRL/ RMII-TXEN | CLK-FANOUT2 | PWM0 | UART1-TX | | PG-EINT12 |
| PG13 | | I/O | I2S1-BCLK | TWI0-SDA | RGMII-CLKIN/ RMII-RXER | PWM2 | LEDC-DO | UART1-RX | | PG-EINT13 |
| PG14 | | I/O | I2S1-DIN0 | TWI2-SCK | MDC | I2S1-DOUT1 | SPI0-WP | UART1-RTS | | PG-EINT14 |
| PG15 | | I/O | I2S1-DOUT0 | TWI2-SDA | MDIO | I2S1-DIN1 | SPI0-HOLD | UART1-CTS | | PG-EINT15 |



4.4 Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

[1].**Signal Name**: The name of every signal.

[2].**Description**: The detailed function description of every signal.

[3].**Type**: Denotes the signal direction:

- I (Input),
- O (Output),
- I/O (Input/Output),
- OD (Open-Drain),
- A (Analog),
- AI (Analog Input),
- AO (Analog Output),
- A I/O (Analog Input/Output),
- P (Power),
- G (Ground)

Table 4-4 Detailed Signal Description

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|------------------------------------|---------------------|
| DRAM | | |
| VDD18-DRAM | DRAM Controller Power Supply | P |
| VCC-DRAM0, VCC-DRAM1 | DRAM Power Supply | P |
| System Control | | |
| BOOT-SEL[1:0] | Boot Media Select | I |
| RESET | Reset Signal (low active) | I, OD |
| Clock | | |
| X32KIN | Clock Input of 32.768 kHz Crystal | AI |
| X32KOUT | Clock Output of 32.768 kHz Crystal | AO |
| VCC-RTC | RTC Power | P |
| VCC-PLL | PLL Power Supply | P |
| DCXO | | |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------------|---|---------------------|
| REFCLK-OUT | Digital Compensated Crystal Oscillator Clock Fanout | AO |
| DXIN | Digital Compensated Crystal Oscillator Input | AI |
| DXOUT | Digital Compensated Crystal Oscillator Output | AO |
| USB | | |
| USB0-DM | USB DRD Data Signal DM | A I/O |
| USB0-DP | USB DRD Data Signal DP | A I/O |
| USB1-DM | USB HOST Data Signal DM | A I/O |
| USB1-DP | USB HOST Data Signal DP | A I/O |
| GPADC | | |
| GPADC0 | General Purpose ADC Input Channel 0 | AI |
| TPADC | | |
| TP-X1 | Touch Panel X1 Input | AI |
| TP-X2 | Touch Panel X2 Input | AI |
| TP-Y1 | Touch Panel Y1 Input | AI |
| TP-Y2 | Touch Panel Y2 Input | AI |
| CVBS OUT | | |
| TVOUT0 | TV CVBS Output | AO |
| VCC-TVOUT | TV CVBS DAC Power | P |
| CVBS IN (Only for F133-B) | | |
| TVIN0 | TV CVBS Input 0 | AI |
| TVIN1 | TV CVBS Input 1 | AI |
| TVIN-VRP | TV CVBS ADC Positive Reference Voltage | P |
| TVIN-VRN | TV CVBS ADC Negative Reference Voltage | P |
| VCC-TVIN | TV CVBS ADC Power | P |
| AUDIO CODEC | | |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|--|---------------------|
| HPOUTR | Headphone Right Output | AO |
| HPOUTL | Headphone Left Output | AO |
| HPOUTFB | Pseudo Differential Headphone Ground Reference | AI |
| HPVCC | Headphone Power | P |
| MICIN3P | Microphone Differential Positive Input 3 | AI |
| MICIN3N | Microphone Differential Negative Input 3 | AI |
| FMINR | FMIN Right Input | AI |
| FMINL | FMIN Left Input | AI |
| LINEINR | LINEIN Right Single-End Input | AI |
| LINEINL | LINEIN Left Single-End Input | AI |
| VRA1 | Internal Reference Voltage | AO |
| VRA2 | Internal Reference Voltage | AO |
| AVCC | Power Supply for Analog Part | P |
| AGND | Analog Ground | G |
| LCD | | |
| LCD-D[23:0] | LCD Data Output | O |
| LCD0-CLK | LCD Clock The pixel data are synchronized by this clock | O |
| LCD0-VSYNC | LCD Vertical Sync It indicates one new frame | O |
| LCD0-HSYNC | LCD Horizontal Sync It indicates one new scan line | O |
| LCD0-DE | LCD Data Output Enable | O |
| TCON-TRIG | LCD Sync (TCON outputs to LCD for sync) | O |
| LVDS | | |
| LVDS0-CKP | LVDS0 Positive Port of Clock | O |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|---|---------------------|
| LVDS0-CKN | LVDS0 Negative Port of Clock | O |
| LVDS0-V[3:0]P | LVDS0 Positive Port of Data Channel [3:0] | O |
| LVDS0-V[3:0]N | LVDS0 Negative Port of Data Channel [3:0] | O |
| LVDS1-CKP | LVDS1 Positive Port of Clock | O |
| LVDS1-CKN | LVDS1 Negative Port of Clock | O |
| LVDS1-V[3:0]P | LVDS1 Positive Port of Data Channel [3:0] | O |
| LVDS1-V[3:0]N | LVDS1 Negative Port of Data Channel [3:0] | O |
| DSI | | |
| DSI-D[3:0]P | DSI Differential Data [3:0] Positive Signal | O |
| DSI-D[3:0]N | DSI Differential Data [3:0] Negative Signal | O |
| DSI-CKP | DSI Differential Clock Positive Signal | O |
| DSI-CKN | DSI Differential Clock Negative Signal | O |
| Parallel CSI | | |
| NCSI0-PCLK | Parallel CSI Pixel Clock | I |
| NCSI0-MCLK | Parallel CSI Master Clock | O |
| NCSI0-HSYNC | Parallel CSI Horizontal Synchronous | I |
| NCSI0-VSYNC | Parallel CSI Vertical Synchronous | I |
| NCSI0-D[7:0] | Parallel CSI Data Bit | I |
| NCSI0-FIELD | Parallel CSI Field Index | I |
| SMHC | | |
| SDC0-CMD | Command Signal for SD Card | I/O, OD |
| SDC0-CLK | Clock for SD Card | O |
| SDC0-D[3:0] | Data Input and Output for SD Card | I/O |
| SDC1-CMD | Command Signal for SDIO WIFI | I/O, OD |
| SDC1-CLK | Clock for SDIO WIFI | O |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|---|---------------------|
| SDC1-D[3:0] | Data Input and Output for SDIO WIFI | I/O |
| SDC2-CMD | Command Signal for eMMC | I/O, OD |
| SDC2-CLK | Clock for eMMC | O |
| SDC2-D[3:0] | Data Input and Output for eMMC | I/O |
| I2S/PCM | | |
| I2S1-MCLK | I2S1 Master Clock | O |
| I2S1-LRCK | I2S1/PCM1 Sample Rate Clock/Sync | I/O |
| I2S1-BCLK | I2S1/PCM1 Bit Rate Clock | I/O |
| I2S1-DOUT[1:0] | I2S1/PCM1 Serial Data Output Channel [1:0] | O |
| I2S1-DIN[1:0] | I2S1/PCM1 Serial Data Input Channel [1:0] | I |
| I2S2-MCLK | I2S2 Master Clock | O |
| I2S2-LRCK | I2S2/PCM2 Sample Rate Clock/Sync | I/O |
| I2S2-BCLK | I2S2/PCM2 Bit Rate Clock | I/O |
| I2S2-DOUT[2:0] | I2S2/PCM2 Serial Data Output Channel [2:0] | O |
| I2S2-DIN[2:0] | I2S2/PCM2 Serial Data Input Channel [2:0] | I |
| DMIC | | |
| DMIC-CLK | Digital Microphone Clock Output | O |
| DMIC-DATA[3:0] | Digital Microphone Data Input | I |
| EMAC | | |
| RGMII-RXD3 | RGMII Receive Data3 | I |
| RGMII-RXD2 | RGMII Receive Data2 | I |
| RGMII-RXD1/RMII-RXD1 | RGMII/RMII Receive Data1 | I |
| RGMII-RXD0/RMII-RXD0 | RGMII/RMII Receive Data0 | I |
| RGMII-RXCK | RGMII Receive Clock | I |
| RGMII-RXCTRL/RMII-CRS-DV | RGMII Receive Control/RMII Carrier Sense Receive Data Valid | I |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|--|---------------------|
| RGMII-CLKIN/RMII-RXER | RGMII Transmit Clock from External/RMII Receive Error | I |
| RGMII-TXD3 | RGMII Transmit Data3 | O |
| RGMII-TXD2 | RGMII Transmit Data2 | O |
| RGMII-TXD1/RMII-TXD1 | RGMII/RMII Transmit Data1 | O |
| RGMII-TXD0/RMII-TXD0 | RGMII/RMII Transmit Data0 | O |
| RGMII-TXCK/RMII-TXCK | RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input | I/O |
| RGMII-TXCTRL/RMII-TXEN | RGMII Transmit Control/RMII Transmit Enable | O |
| MDC | RGMII/RMII Management Data Clock | O |
| MDIO | RGMII/RMII Management Data Input/Output | I/O |
| EPHY-25M | 25 MHz Output for EMAC PHY | O |
| OWA | | |
| OWA-IN | One Wire Audio Input | I |
| OWA-OUT | One Wire Audio Output | O |
| LEDC | | |
| LEDC-DO | Intelligent Control LED Signal Output | O |
| Interrupt | | |
| PB-EINT[7:2] | GPIO B Interrupt | I |
| PC-EINT[7:2] | GPIO C Interrupt | I |
| PD-EINT[22:0] | GPIO D Interrupt | I |
| PE-EINT[13:0] | GPIO E Interrupt | I |
| PF-EINT[6:0] | GPIO F Interrupt | I |
| PG-EINT[15:0] | GPIO G Interrupt | I |
| CIR Receiver | | |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|--|---------------------|
| IR-RX | Consumer Infrared Receiver | I |
| CIR Transmitter | | |
| IR-TX | Consumer Infrared Transmitter | O |
| PWM | | |
| PWM[7:0] | Pulse Width Modulation Output Channel [7:0] | I/O |
| SPI&SPI_DBI | | |
| SPI0-CS | SPI0 Chip Select Signal, Low Active | I/O |
| SPI0-CLK | SPI0 Clock Signal Provides serial interface timing. | I/O |
| SPI0-MOSI | SPI0 Master Data Out, Slave Data In | I/O |
| SPI0-MISO | SPI0 Master Data In, Slave Data Out | I/O |
| SPI0-WP | SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. | I/O |
| SPI0-HOLD | SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. | I/O |
| SPI1-CS | SPI1 Chip Select Signal, Low Active | I/O |
| SPI1-CLK | SPI1 Clock Signal Provides serial interface timing. | I/O |
| SPI1-MOSI | SPI1 Master Data Out, Slave Data In | I/O |
| SPI1-MISO | SPI1 Master Data In, Slave Data Out | I/O |
| SPI1-WP | SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output | I/O |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|---|---------------------|
| | for SPI Quad Input or Quad Output mode. | |
| SPI1-HOLD | SPI1 Hold Signal Pauses any serial communication with the device without resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. | I/O |
| DBI-CSX | Chip Select Signal, Low Active | I/O |
| DBI-SCLK | Serial Clock Signal | I/O |
| DBI-SDO | Data Output Signal | I/O |
| DBI-SDI | Data Input Signal The data is sampled on the rising edge and the falling edge | I/O |
| DBI-TE | Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable. | I/O |
| DBI-DCX | DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter. | I/O |
| DBI-WRX | When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data | I/O |
| UART | | |
| UART0-TX | UART0 Data Transmit | O |
| UART0-RX | UART0 Data Receive | I |
| UART1-TX | UART1 Data Transmit | O |
| UART1-RX | UART1 Data Receive | I |
| UART1-CTS | UART1 Data Clear to Send | I |
| UART1-RTS | UART1 Data Request to Send | O |
| UART2-TX | UART2 Data Transmit | O |
| UART2-RX | UART2 Data Receive | I |

| Signal Name ^[1] | Description ^[2] | Type ^[3] |
|----------------------------|----------------------------|---------------------|
| UART2-CTS | UART2 Data Clear to Send | I |
| UART2-RTS | UART2 Data Request to Send | O |
| UART3-TX | UART3 Data Transmit | O |
| UART3-RX | UART3 Data Receive | I |
| UART3-CTS | UART3 Data Clear to Send | I |
| UART3-RTS | UART3 Data Request to Send | O |
| UART4-TX | UART4 Data Transmit | O |
| UART4-RX | UART4 Data Receive | I |
| UART5-TX | UART5 Data Transmit | O |
| UART5-RX | UART5 Data Receive | I |
| TWI | | |
| TWI0-SCK | TWI0 Serial Clock Signal | I/O |
| TWI0-SDA | TWI0 Serial Data Signal | I/O |
| TWI1-SCK | TWI1 Serial Clock Signal | I/O |
| TWI1-SDA | TWI1 Serial Data Signal | I/O |
| TWI2-SCK | TWI2 Serial Clock Signal | I/O |
| TWI2-SDA | TWI2 Serial Data Signal | I/O |
| TWI3-SCK | TWI3 Serial Clock Signal | I/O |
| TWI3-SDA | TWI3 Serial Data Signal | I/O |
| JTAG | | |
| R-JTAG-MS | RISC JTAG Mode Select | I |
| R-JTAG-CK | RISC JTAG Clock Signal | I |
| R-JTAG-DO | RISC JTAG Data Output | O |
| R-JTAG-DI | RISC JTAG Data Input | I |

5 Electrical Characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at $T_a = 25\text{ }^\circ\text{C}$ and $T_a = T_a\text{ max}$.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on $T_a = 25\text{ }^\circ\text{C}$. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.



Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

| Symbol | Parameter | Min ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|--------|-----------|--------------------|--------------------|------|
|--------|-----------|--------------------|--------------------|------|

| Symbol | Parameter | Min ⁽¹⁾ | Max ⁽¹⁾ | Unit | |
|------------------------------------|---|---|--------------------|------|---|
| AVCC | Power Supply for Analog Part | -0.3 | 2.16 | V | |
| HPVCC | Headphone Power | -0.3 | 2.16 | V | |
| VCC-PD | Digital GPIO D Power | -0.3 | 3.96 | V | |
| VCC-PE | Digital GPIO E Power | -0.3 | 3.96 | V | |
| VCC-PG | Digital GPIO G Power | -0.3 | 3.96 | V | |
| VCC-IO | Power Supply for 3.3 V Digital Part | -0.3 | 3.96 | V | |
| VCC-RTC | Power Supply for RTC | -0.3 | TBD | V | |
| VCC-PLL | Power Supply for System PLL | -0.3 | TBD | V | |
| VCC-LVDS | Power Supply for LVDS | -0.3 | TBD | V | |
| VCC-TVOUT | Power Supply for TVOUT | -0.3 | TBD | V | |
| VCC-TVIN | Power Supply for TVIN | -0.3 | TBD | V | |
| VCC-DRAM0, VCC-DRAM1 | Power Supply for DRAM IO and DDR2 | -0.3 | TBD | V | |
| VDD18-DRAM | Power Supply for DRAM Controller | -0.3 | TBD | V | |
| VDD-CORE0, VDD-CORE1 | Power Supply for CPU and System | -0.3 | TBD | V | |
| VDD-SYS0, VDD-SYS1, VDD-SYS2 | Power Supply for System | -0.3 | TBD | V | |
| LDO-IN | Internal LDOA/B Input Voltage | -0.3 | 3.96 | V | |
| LDOA-OUT | Internal LDOA Output Voltage for Analog Device and IO | -0.3 | 2.16 | V | |
| LDOB-OUT | Internal LDOB Output Voltage for VCC-DRAM | -0.3 | 2.16 | V | |
| T _{STG} | Storage Temperature | -40 | 150 | °C | |
| T _j | Working Junction Temperature | -20 | 125 | °C | |
| V _{ESD} | Electrostatic Discharge ⁽²⁾ | Human Body Model (HBM) ⁽³⁾ | -4000 | 4000 | V |
| | | Charged Device Model (CDM) ⁽⁴⁾ | -500 | 500 | V |

| Symbol | Parameter | Min ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|-----------------------|---|--------------------|--------------------|------|
| I _{Latch-up} | Latch-up I-test performance current-pulse injection on each IO pin ⁽⁵⁾ | Pass | | |
| | Latch-up over-voltage performance voltage injection on each IO pin ⁽⁶⁾ | Pass | | |

- (1) The min/max voltages of power rails are guaranteed by design, not tested in production.
- (2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.
- (3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
- (4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
- (5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.
- (6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x V_{ddmax} at room temperature.

5.3 Recommended Operating Conditions

Table 5-2 describes operating conditions of the F133.



NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|--|-------|-----|--------------------|------|
| T _a | Ambient Operating Temperature (when VCC-DRAM0/1 uses external power) | -20 | - | 85 | °C |
| | Ambient Operating Temperature (when VCC-DRAM0/1 uses internal LDO) | -20 | - | 70 | °C |
| T _j | Working Junction Temperature Range | -20 | - | 110 ⁽¹⁾ | °C |
| AVCC | Power Supply for Analog Part | 1.782 | 1.8 | 1.818 | V |
| HPVCC | Headphone Power | 1.782 | 1.8 | 1.818 | V |
| VCC-PD | Digital GPIO D Power 1.8 V voltage | 1.62 | 1.8 | 1.98 | V |

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------------------|---|-------|---------------------|-------|------|
| | 3.3 V voltage | 2.97 | 3.3 | 3.63 | |
| VCC-PE | Digital GPIO E Power | | | | |
| | 1.8 V voltage | 1.62 | 1.8 | 1.98 | V |
| | 2.8 V voltage | 2.52 | 2.8 | 3.08 | |
| | 3.3 V voltage | 2.97 | 3.3 | 3.63 | |
| | | | | | |
| VCC-PG | Digital GPIO G Power | | | | |
| | 1.8 V voltage | 1.62 | 1.8 | 1.98 | V |
| | 3.3 V voltage | 2.97 | 3.3 | 3.63 | |
| | | | | | |
| VCC-IO | Power Supply for Digital Part | | | | |
| | 3.3 V voltage | 2.97 | 3.3 | 3.63 | V |
| VCC-RTC | Power Supply for RTC | TBD | 1.8 | TBD | V |
| VCC-PLL | Power Supply for System PLL | TBD | 1.8 | TBD | V |
| VCC-LVDS | Power Supply for LVDS | TBD | 1.8 | TBD | V |
| VCC-TVOUT | Power Supply for TVOUT | TBD | 3.3 | TBD | V |
| VCC-TVIN | Power Supply for TVIN | TBD | 1.8 | TBD | V |
| VCC-DRAM0, VCC-DRAM1 | Power Supply for DRAM IO and DDR2 | TBD | 1.8 | TBD | V |
| VDD18-DRAM | Power Supply for DRAM Controller | 1.7 | 1.8 | 1.95 | V |
| VDD-CORE0, VDD-CORE1 | Power Supply for CPU and System | TBD | 0.9 | TBD | V |
| VDD-SYS0, VDD-SYS1, VDD-SYS2 | Power Supply for System | TBD | 0.9 | TBD | V |
| LDO-IN | Internal LDOA/B Input Voltage | 2.4 | 3.3 | 3.6 | V |
| LDOA-OUT | Internal LDOA Output Voltage for Analog Device and IO | 1.782 | 1.8 | 1.818 | V |
| LDOB-OUT | Internal LDOB Output Voltage for VCC-DRAM | 1.31 | 1.35 ⁽²⁾ | 1.39 | V |
| | | 1.455 | 1.5 | 1.545 | |
| | | 1.746 | 1.8 | 1.854 | |

- (1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.
- (2). The default voltage of LDOB-OUT is 1.35 V.

5.4 Power Consumption Parameters

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in the following table.



NOTE

Since the data presented in the following table is based on empirical measurements on small sample size, the results presented are not guaranteed.

Table 5-3 Power Consumption Parameters

| Parameter | Sub Parameter | Power Supply | Condition | Typ | Max | Unit |
|---------------------|---------------|--|-------------------------------|-----|-----|------|
| Internal Core Power | CPU | VDD-CORE0, VDD-CORE1 | 0.9 V | - | TBD | mA |
| | SYS | VDD-SYS0, VDD-SYS1, VDD-SYS2, VDD-CORE0, VDD-CORE1 | 0.9 V | - | TBD | mA |
| GPIO Power | | VCC-IO | For GPIO, voltage 3.3 V, N=19 | - | 114 | mA |
| | | VCC-PD | For GPIO, voltage 3.3 V, N=23 | - | 138 | mA |
| | | VCC-PE | For GPIO, voltage 3.3 V, N=14 | - | 84 | mA |
| | | VCC-PG | For GPIO, voltage 3.3 V, N=16 | - | 96 | mA |
| Memory I/O Power | | VCC-DRAM | SIP 64 MB DDR2 | - | TBD | mA |
| LVDS Power | | VCC-LVDS | 1.8 V, 700 MHz dual link | - | 50 | mA |
| CVBS OUT Power | | VCC-TVOUT | 3.3 V | - | TBD | mA |
| CVBS IN Power | | VCC-TVIN | 1.8 V | - | TBD | mA |

| Parameter | Sub Parameter | Power Supply | Condition | Typ | Max | Unit |
|-------------------|---------------|--------------|---|-----|------|------|
| 24 MHz Oscillator | Crystal | VCC-PLL | 1.8 V | - | 2 | mA |
| RTC Power | | VCC-RTC | 1.8 V | - | 0.01 | mA |
| ADC Analog Power | | AVCC | 1.8 V, 48 kHz sample rate, 5-chs are enabled | - | TBD | mA |
| DAC Analog Power | | AVCC | 1.8 V, 48 kHz sample rate, 2-chs are enabled | - | TBD | mA |
| USB Power | | VCC-IO | 2 x USB, 3.3 V | - | 35 | mA |

General equation for estimated, maximum power consumption of an group IO power supply:

$$I_{max} = N \times 6 \text{ mA}$$

Where:

N—Number of IO pins supplied by the power line.

The maximum power consumption for each IO is 6 mA.

5.5 DC Electrical Characteristics

Table 5-4 summarizes the DC electrical characteristics of the F133. For the interfaces of GPIO function port, refer to the DC parameters in Table 5-4 unless otherwise stated.

Table 5-4 DC Electrical Characteristics
(VCC-IO/VCC-PD/VCC-PE/VCC-PG)

| Symbol | Parameter | Min | Typ | Max | Unit | |
|-----------------|----------------------------|----------------------|-----|--------------|------|----|
| V _{IH} | High-Level Input Voltage | 0.7 * VCC-IO | - | VCC-IO + 0.3 | V | |
| V _{IL} | Low-Level Input Voltage | -0.3 | - | 0.3 * VCC-IO | V | |
| R _{PU} | Input Pull-up Resistance | PC3 to PC7, PF3, PF6 | 12 | 15 | 18 | kΩ |
| | | PG0 to PG5 | 26 | 33 | 40 | kΩ |
| | | Other GPIOs | 80 | 100 | 120 | kΩ |
| R _{PD} | Input Pull-down Resistance | PC3 to PC7, PF3, PF6 | 12 | 15 | 18 | kΩ |
| | | PG0 to PG5 | 26 | 33 | 40 | kΩ |

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|----------------------------------|-------------------|-----|-------------|------|
| | Other GPIOs | 80 | 100 | 120 | kΩ |
| I_{IH} | High-Level Input Current | - | - | 10 | uA |
| I_{IL} | Low-Level Input Current | - | - | 10 | uA |
| V_{OH} | High-Level Output Voltage | $V_{CC-IO} - 0.3$ | - | V_{CC-IO} | V |
| V_{OL} | Low-Level Output Voltage | 0 | - | 0.2 | V |
| I_{OZ} | Tri-State Output Leakage Current | -10 | - | 10 | uA |
| C_{IN} | Input Capacitance | - | - | 5 | pF |
| C_{OUT} | Output Capacitance | - | - | 5 | pF |

5.6 SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

Figure 5-1 SDIO Voltage Waveform

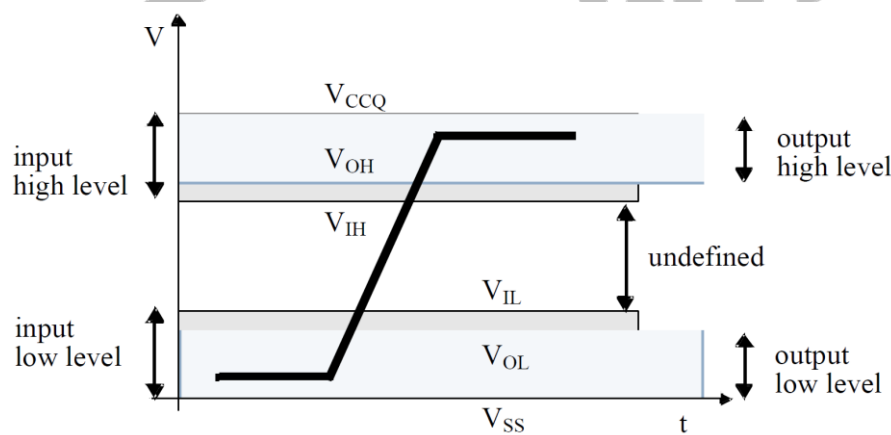


Table 5-5 shows 3.3 V SDIO electrical parameters.

Table 5-5 3.3 V SDIO Electrical Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|---------------------------|------------------|-----|-------------------|------|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| V_{CCQ} | I/O voltage | 2.7 | - | 3.6 | V |
| V_{OH} | Output high-level voltage | $0.75 * V_{CCQ}$ | - | - | V |
| V_{OL} | Output low-level voltage | - | - | $0.125 * V_{CCQ}$ | V |

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|--------------------------|--------------------------|-----|-------------------------|------|
| V _{IH} | Input high-level voltage | 0.625 * V _{CCQ} | - | V _{CCQ} + 0.3 | V |
| V _{IL} | Input low-level voltage | V _{SS} - 0.3 | - | 0.25 * V _{CCQ} | V |

Table 5-6 shows 1.8 V SDIO electrical parameters.

Table 5-6 1.8 V SDIO Electrical Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|--|------|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| V _{CCQ} | I/O voltage | 1.7 | - | 1.95 | V |
| V _{OH} | Output high-level voltage | V _{CCQ} - 0.45 | - | - | V |
| V _{OL} | Output low-level voltage | - | - | 0.45 | V |
| V _{IH} | Input high-level voltage | 0.625 * V _{CCQ} ⁽¹⁾ | - | V _{CCQ} + 0.3 | V |
| V _{IL} | Input low-level voltage | V _{SS} - 0.3 | - | 0.35 * V _{CCQ} ⁽²⁾ | V |
| (1).0.7 * V _{CCQ} for MMC4.3 or lower. (2).0.3 * V _{CCQ} for MMC4.3 or lower. | | | | | |

5.7 GPADC Electrical Characteristics

The GPADC contains a 1-ch analog-to-digital (ADC) converter. The GPADC is a type of successive approximation register (SAR) converter. Table 5-7 lists GPADC electrical characteristics.

Table 5-7 GPADC Electrical Characteristics

| Parameter | Min | Typ | Max | Unit |
|------------------------|-----|-----|------|------------------|
| ADC Resolution | - | 12 | - | bits |
| Full-scale Input Range | 0 | - | AVCC | V |
| Quantizing Error | - | 8 | - | LSB |
| Clock Frequency | - | - | 1 | MHz |
| Conversion Time | - | 14 | - | ADC Clock Cycles |

5.8 Audio Codec Electrical Characteristics

Test Conditions:

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, Input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-8 Audio Codec Typical Performance Parameters

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|-----------------------------------|---|-----|-----|------|------|
| DAC Path | DAC to HPOUTL or HPOUTR | | | | | |
| | Full-scale | 0dBFS 1 kHz | - | 540 | - | Vrms |
| | SNR (A-weighted) | Odata | - | 95 | - | dB |
| | THD+N | 0dBFS 1 kHz | - | -85 | - | dB |
| | Crosstalk | R_0dB_L_Odata 1 kHz L_0dB_R_Odata 1 kHz | - | TBD | - | dB |
| ADC Path | LINEINLR via ADC | | | | | |
| | Output Level | 1.7 Vpp, 1 kHz | - | 875 | - | mFFS |
| | SNR (A-weighted) | 0 Vpp | - | 94 | - | dB |
| | THD+N | 1.7 Vpp, 1 kHz | - | -88 | - | dB |
| | FMINLR via ADC | | | | | |
| | Output Level | 1.7 Vpp, 1 kHz | - | 875 | - | mFFS |
| | SNR (A-weighted) | 0 Vpp | - | 94 | - | dB |
| | THD+N | 1.7 Vpp, 1 kHz | - | -88 | - | dB |
| | MICIN via ADC | | | | | |
| | Output Level | MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 0 dB Gain | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 98 | - | dB |
| | THD+N | | - | -90 | - | dB |
| | Output Level | MICP=1.695Vpp/2, MICN=1.695Vpp/2, 1 kHz, 6 dB Gain | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 97 | - | dB |
| | THD+N | | - | -93 | - | dB |
| Output Level | MICP=0.788Vpp/2, MICN=0.788Vpp/2, | - | 880 | - | mFFS | |

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|------------------|--|-----|-----|-----|------|
| | SNR (A-weighted) | 1 kHz, 12 dB Gain | - | 94 | - | dB |
| | THD+N | | - | -85 | - | dB |
| | Output Level | MICP=0.392Vpp/2, MICN=0.392Vpp/2, 1 kHz, 18 dB Gain | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 92 | - | dB |
| | THD+N | | - | -83 | - | dB |
| | Output Level | | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 87 | - | dB |
| | THD+N | MICP=0.197Vpp/2, MICN=0.197Vpp/2, 1 kHz, 24 dB Gain | - | -80 | - | dB |
| | Output Level | | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 82 | - | dB |
| | THD+N | MICP=0.101Vpp/2, MICN=0.101Vpp/2, 1 kHz, 30 dB Gain | - | -73 | - | dB |
| | Output Level | | - | 880 | - | mFFS |
| | SNR (A-weighted) | | - | 76 | - | dB |
| | THD+N | | - | -65 | - | dB |

5.9 External Clock Source Characteristics

5.9.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-9 High-speed 24 MHz Crystal Circuit Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|---|-------------|-----|-----|------|
| f_{X24M_IN} | Crystal parallel resonance frequency | - | 24 | - | MHz |
| | Crystal frequency stability and tolerance at 25 °C ⁽¹⁾ | -50 | - | +50 | ppm |
| | Oscillation mode | Fundamental | | | - |
| C_0 | Shunt capacitance ⁽²⁾ | - | 6.5 | - | pF |

1. The 50 ppm frequency stability and tolerance can meet the requirement of F133. We recommend

selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.

- The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-10 Crystal Circuit Parameters

| Symbol | Parameter |
|-------------|--|
| C_1 | C_1 capacitance |
| C_2 | C_2 capacitance |
| C_L | Equivalent load capacitance, specified by the crystal manufacturer |
| C_0 | Crystal shunt capacitance, specified by the crystal manufacturer |
| C_{shunt} | Total shunt capacitance |

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1 , C_2 , and C_{shunt} .

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.



NOTE

For the above capacitances of 24 MHz crystal circuit, refer to the capacitance recommended in the [F133_Schematic_Diagram](#).

5.9.2 Low-speed Crystal/Ceramic Resonator Characteristics

The F133 contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the

software.

The F133 also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-11 Low-speed 32.768 kHz Crystal Circuit Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|---|-------------|--------|-----|------|
| f_{X32K_IN} | Crystal parallel resonance frequency | - | 32.768 | - | kHz |
| | Crystal frequency stability and tolerance at 25 °C ⁽¹⁾ | - | - | - | ppm |
| | Oscillation mode | Fundamental | | | - |
| C_0 | Shunt capacitance ⁽²⁾ | - | 1.1 | - | pF |

1. The F133 has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.
2. The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.



NOTE

For capacitances of 32.768 kHz crystal circuit, refer to the capacitance recommended in the [F133_Schematic_Diagram](#).

5.10 Internal Reset Electrical Characteristics

Table 5-12 Internal Reset Electrical Characteristics

| Parameter | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------------|------|-----|---------|------|
| Power-on threshold voltage of VDD-SYS on which the reset signal is excited | Ta= -20°C to 85°C | - | 0.4 | - | V |
| Reset active timeout period | Ta= -20°C to 85°C | - | 64 | - | ms |
| Reset open-drain output voltage | Ta= -20°C to 85°C, pull up 3.3 V | -0.3 | - | 0.3*VCC | V |

5.11 External Memory Electrical Characteristics

5.11.1 SMHC AC Electrical Characteristics

5.11.1.1 HS-SDR Mode



NOTE

IO voltage is 1.8 V or 3.3 V.

Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram

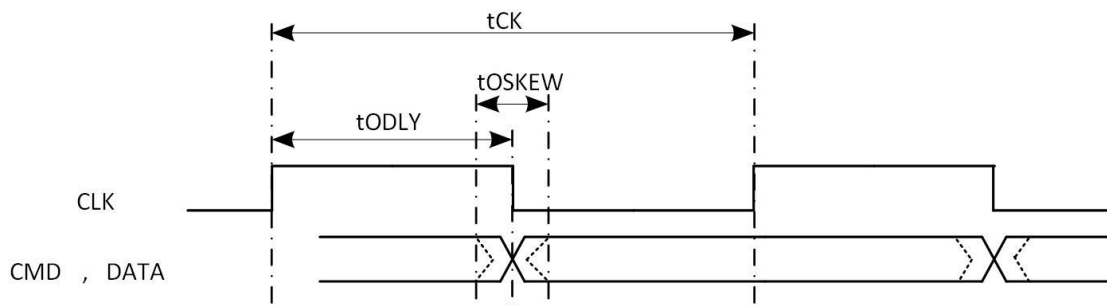


Table 5-13 SMHC HS-SDR Mode Output Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|------|-----|------|
| CLK | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Output CMD, DATA (referenced to CLK) | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI |
| Data output delay skew time | tOSKEW | 0.5 | - | 0.8 | ns |
| <p>(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.</p> <p>(2). The driver strength level of GPIO is 2 for test.</p> | | | | | |

Figure 5-3 SMHC HS-SDR Mode Input Timing Diagram

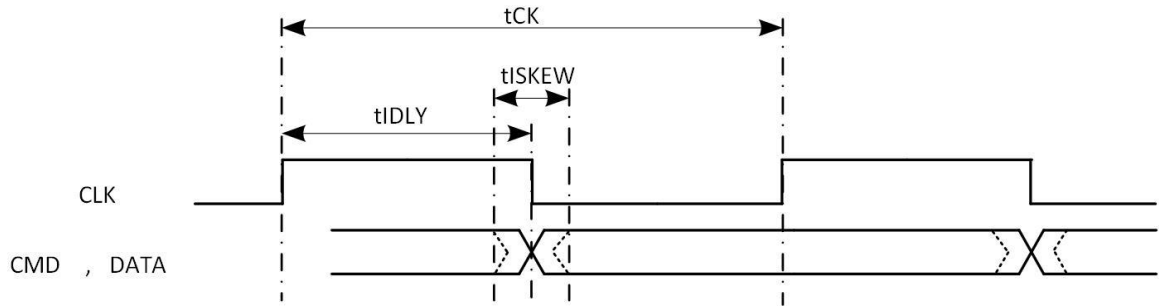


Table 5-14 SMHC HS-SDR Mode Input Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----|-----|------|
| CLK | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Input CMD, DATA (referenced to CLK 50 MHz) | | | | | |
| Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay | tIDLY | - | - | - | ns |
| Data input skew time in SDR mode | tISKEW | 0.5 | - | 0.8 | ns |
| (1). The driver strength level of GPIO is 2 for test. | | | | | |

5.11.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

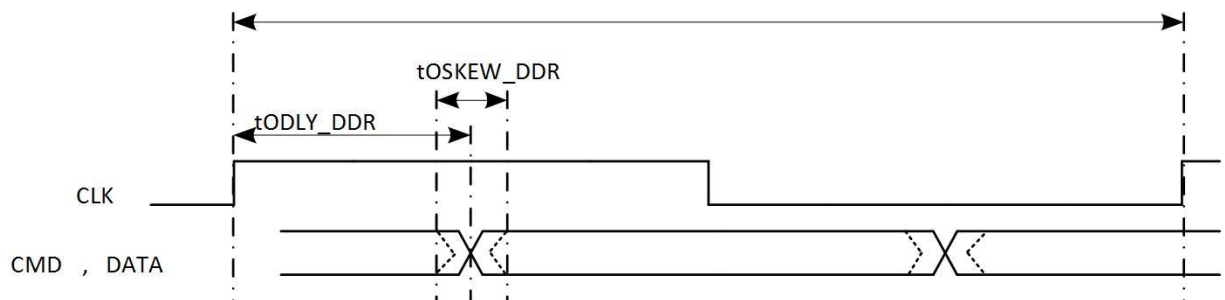


Table 5-15 SMHC HS-DDR Mode Output Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|------|------|------|
| CLK | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Output CMD, DATA (referenced to CLK) | | | | | |
| CMD, Data output delay time in DDR mode | tODLY_DDR | - | 0.25 | 0.25 | UI |
| Data output delay skew time | tOSKEW_DDR | 0.5 | - | 0.8 | ns |
| <p>(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.</p> <p>(2). The driver strength level of GPIO is 2 for test.</p> | | | | | |

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

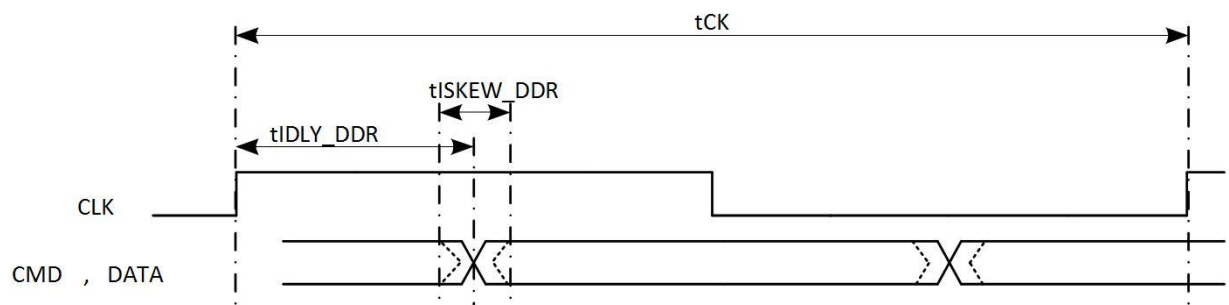


Table 5-16 SMHC HS-DDR Mode Input Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|-----|-----|------|
| CLK | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Input CMD, DATA (referenced to CLK 50 MHz) | | | | | |
| Data input delay in DDR mode. It includes Clock's PCB delay time, Data's | tIDLY_DDR | - | - | - | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|-----|-----|------|
| PCB delay time and device's data output delay | | | | | |
| Data input skew time in DDR mode | tISKEW_DDR | 0.5 | - | 0.8 | ns |

(1). The driver strength level of GPIO is 2 for test.

5.11.1.3 HS200 Mode

Figure 5-6 SMHC HS200 Mode Output Timing Diagram

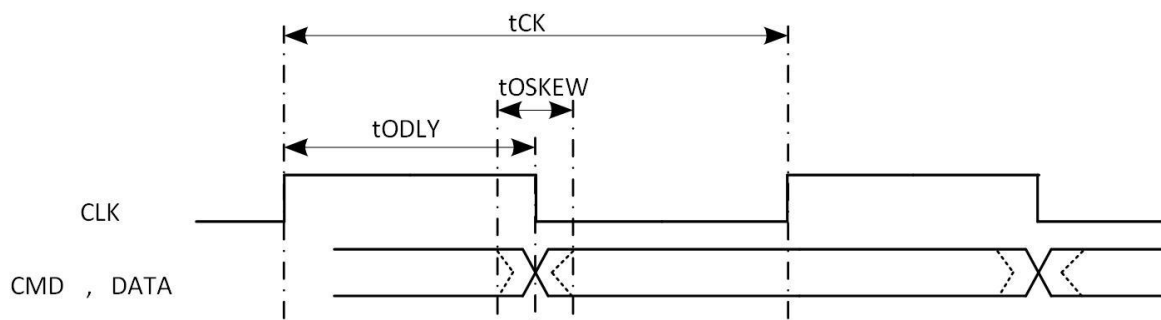


Table 5-17 SMHC HS200 Mode Output Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|------|-----|------|
| CLK | | | | | |
| Clock frequency | tCK | 0 | - | 150 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Output CMD, DATA (referenced to CLK) | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI |
| Data output delay skew time | tOSKEW | 0.5 | - | 0.8 | ns |

(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.
 (2). The driver strength level of GPIO is 3 for test.

Figure 5-7 SMHC HS200 Mode Input Timing Diagram

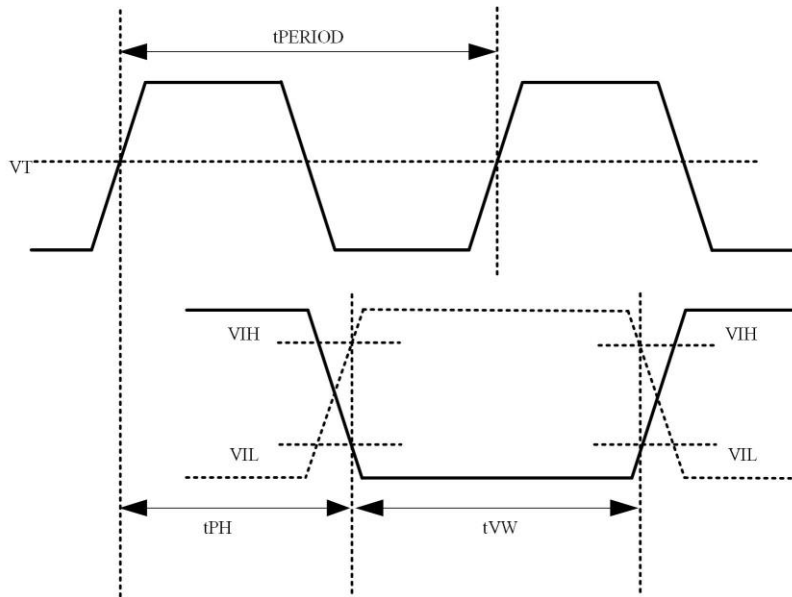


Table 5-18 SMHC HS200 Mode Input Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|--|-----------------------|---------------------|-----|---------------------|------|-----------------|
| CLK | | | | | | |
| Clock period | t_{PERIOD} | 6.66 | - | - | ns | Max: 150 MHz |
| Duty cycle | DC | 45 | 50 | 55 | % | |
| Rise time, fall time | t_{TLH} , t_{THL} | - | - | 0.2 | UI | |
| Input CMD, DATA (referenced to CLK) | | | | | | |
| Input delay | t_{PH} | 0 | - | 2 | UI | |
| Input delay variation due to temperature change after tuning | d_{PH} | -350 ^[3] | - | 1550 ^[4] | ps | |
| CMD, Data valid window | t_{VW} | 0.575 | - | - | UI | |
| <p>(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.</p> <p>(2). The driver strength level of GPIO is 3 for test.</p> <p>(3). Temperature variation: -20°C.</p> | | | | | | |

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|-----------------------------------|--------|-----|-----|-----|------|--------|
| (4). Temperature variation: 90°C. | | | | | | |

5.12 External Peripheral Electrical Characteristics

5.12.1 LCD AC Electrical Characteristics

Figure 5-8 HV_IF Interface Vertical Timing

Vertical Timing

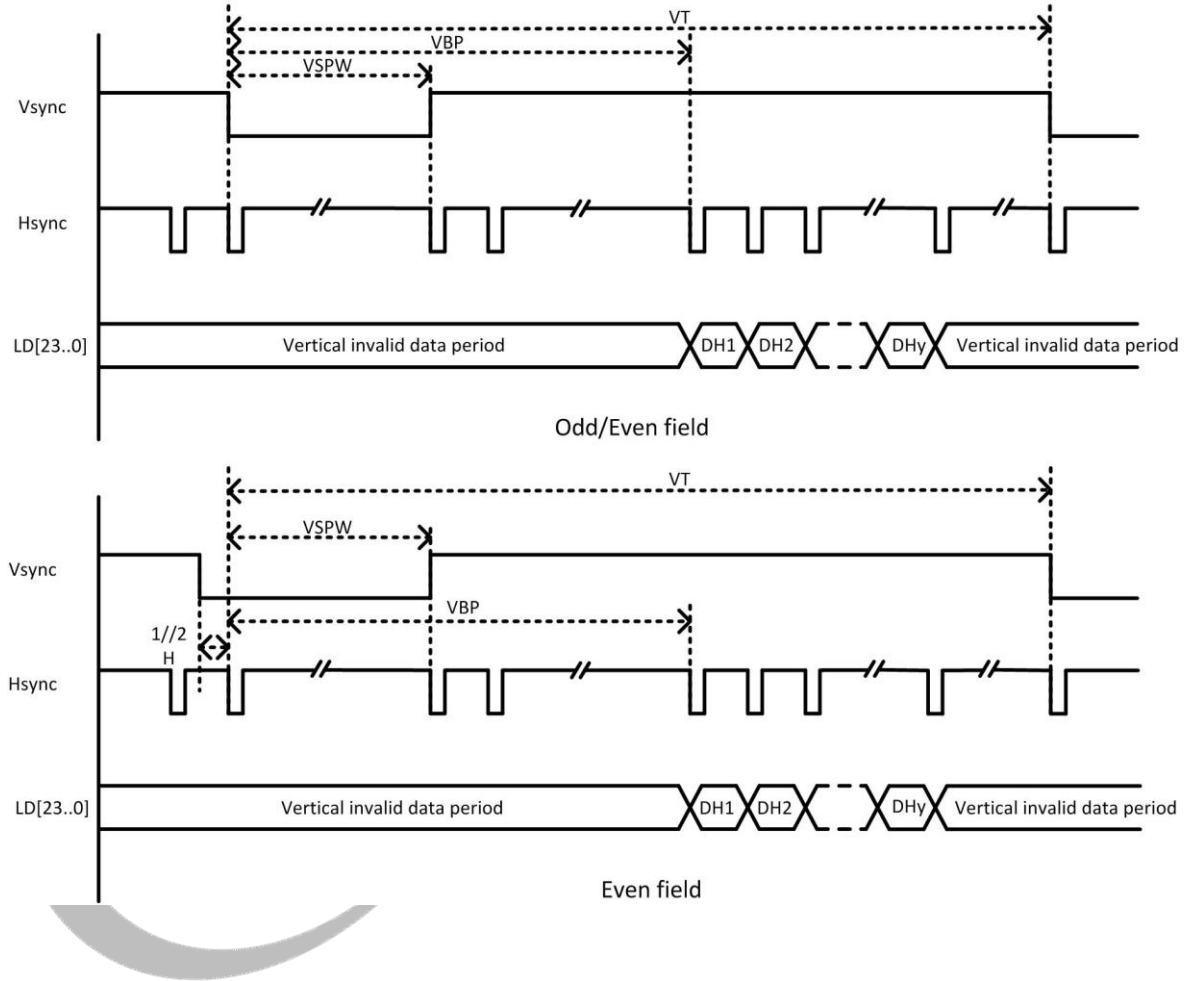


Figure 5-9 HV_IF Interface Horizontal Timing

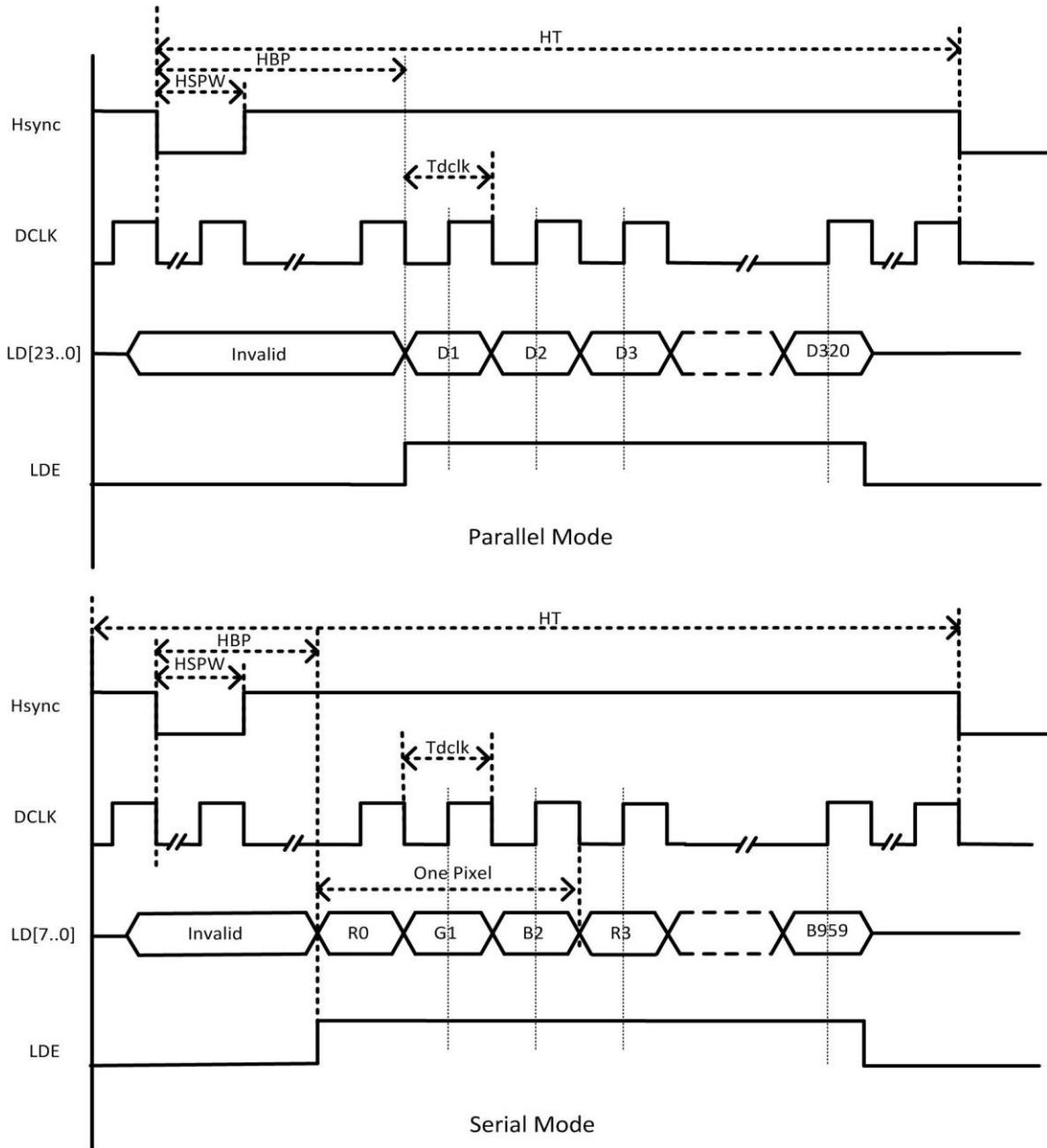


Table 5-19 LCD HV_IF Interface Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|-------------------|--------|-----|--------|-----|-------|
| DCLK cycle time | tDCLK | 5 | - | - | ns |
| Hsync period time | tHT | - | HT+1 | - | tDCLK |
| Hsync width | tHSPW | - | HSPW+1 | - | tDCLK |
| Hsync back porch | tHBP | - | HBP+1 | - | tDCLK |
| Vsync period time | tVT | - | VT/2 | - | tHT |
| Vsync width | tVSPW | - | VSPW+1 | - | tHT |

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------|--------|-----|-------|-----|------|
| Vsync back porch | tVBP | - | VBP+1 | - | tHT |

(1) Vsync: Vertical sync, indicates one new frame.
 (2) Hsync: Horizontal sync, indicates one new scan line.
 (3) DCLK: Dot clock, pixel data are sync by this clock.
 (4) LDE: LCD data enable.
 (5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

5.12.2 CSI AC Electrical Characteristics

Figure 5-10 CSI Data Sample Timing

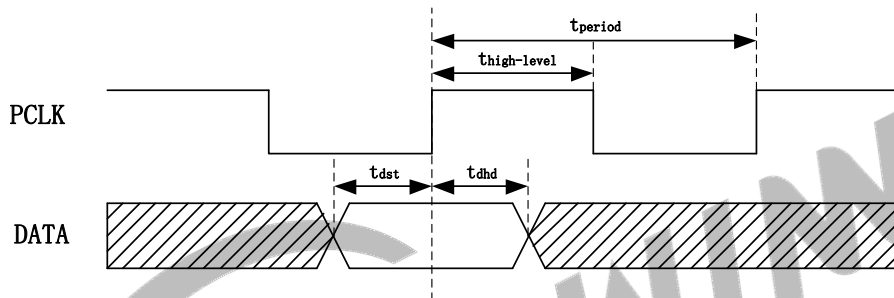


Table 5-20 CSI Interface Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------------------------|------|-----|-------|------|
| Pclk period | t_{period} | 6.73 | - | - | ns |
| Pclk frequency | $1/t_{period}$ | - | - | 148.5 | MHz |
| Pclk duty | $t_{high-level}/t_{period}$ | 40 | 50 | 60 | % |
| Data input setup time | t_{dst} | 0.6 | - | - | ns |
| Data input hold time | t_{dhd} | 0.6 | - | - | ns |

5.12.3 EMAC AC Electrical Characteristics

5.12.3.1 RGMII

Figure 5-11 RGMII Interface Transmit Timing

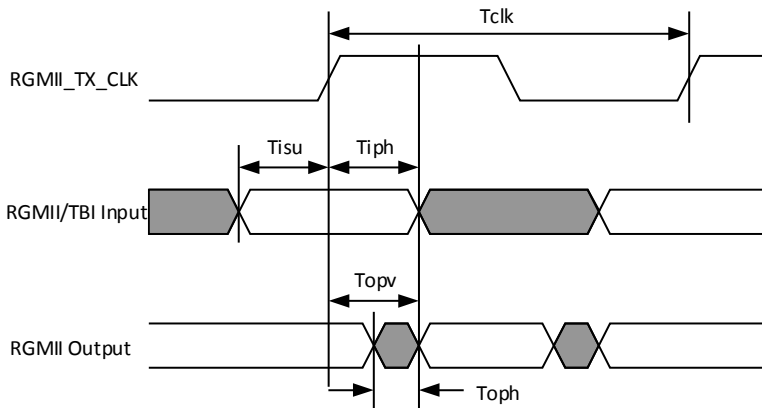


Table 5-21 RGMII Transmit Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----|------|------|
| RGMII_TX_CLK clock period | Tclk | 8 | - | DC | ns |
| RGMII/TBI input setup prior to RGMII_TX_CLK | Tisu | 2.8 | - | - | ns |
| RGMII/TBI input data hold after RGMII_TX_CLK | Tiph | 0.1 | - | - | ns |
| RGMII output data valid after RGMII_TX_CLK | Topv | - | - | 0.85 | ns |
| RGMII output data hold after RGMII_TX_CLK | Toph | 0 | - | - | ns |

Figure 5-12 RGMII Interface Receive Timing

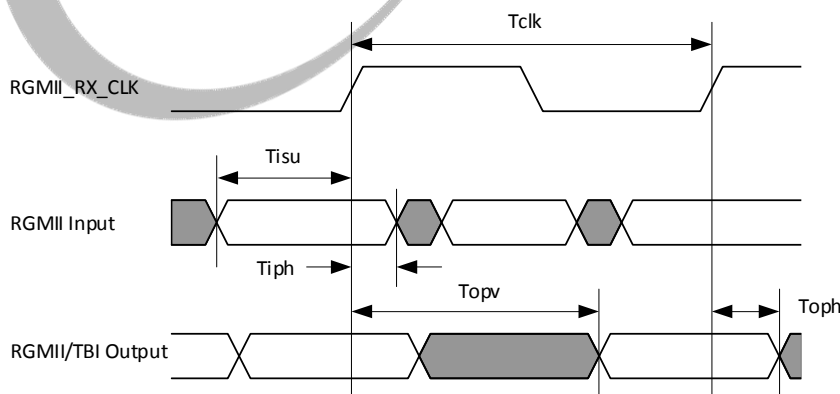


Table 5-22 RGMII Receive Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------|--------|-----|-----|-----|------|
|-----------|--------|-----|-----|-----|------|

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|-----|-----|------|
| RGMII_RX_CLK clock period | Tclk | 8 | - | DC | ns |
| RGMII input setup prior to RGMII_RX_CLK | Tisu | 2.6 | - | - | ns |
| RGMII input data hold after RGMII_RX_CLK | Tiph | 0.8 | - | - | ns |
| RGMII/TBI input data valid after RGMII_RX_CLK | Topv | - | - | 5.2 | ns |
| RGMII output data hold after RGMII_RX_CLK | Toph | 0.1 | - | - | ns |
| TBI output data hold after RGMII_RX_CLK | | 0.5 | - | - | |

5.12.3.2 RMII

Figure 5-13 RMII Interface Transmit Timing

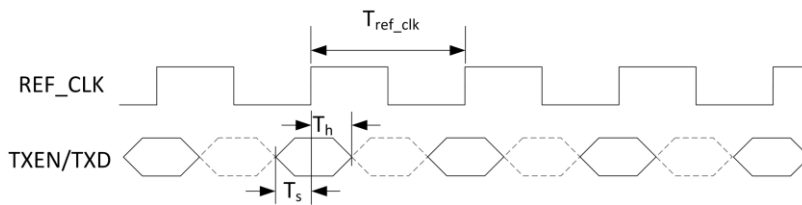


Table 5-23 RMII Transmit Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------|----------------|-----|-----|-----|------|
| Reference clock period | T_{ref_clk} | - | 20 | - | ns |
| TXD/TXEN to REF_CLK setup time | T_s | 4 | - | - | ns |
| TXD/TXEN to REF_CLK hold time | T_h | 2 | - | - | ns |

Figure 5-14 RMII Interface Receive Timing

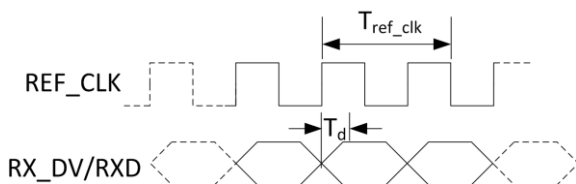


Table 5-24 RMII Receive Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------|----------------|-----|-----|-----|------|
| Reference clock period | T_{ref_clk} | - | 20 | - | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------------------|--------|-----|-----|-----|------|
| REF_CLK rising edge to RX_DV/RXD | Td | - | 10 | 12 | ns |

5.12.4 SPI AC Electrical Characteristics

Figure 5-15 SPI Writing Timing

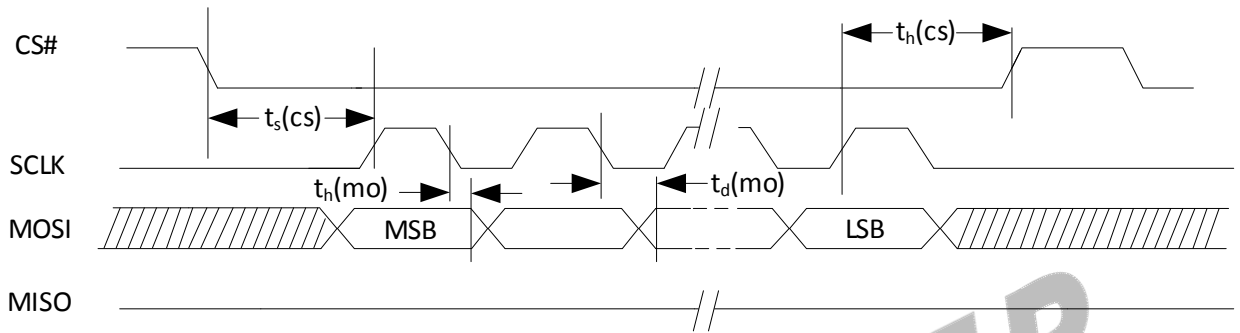


Figure 5-16 SPI Reading Timing

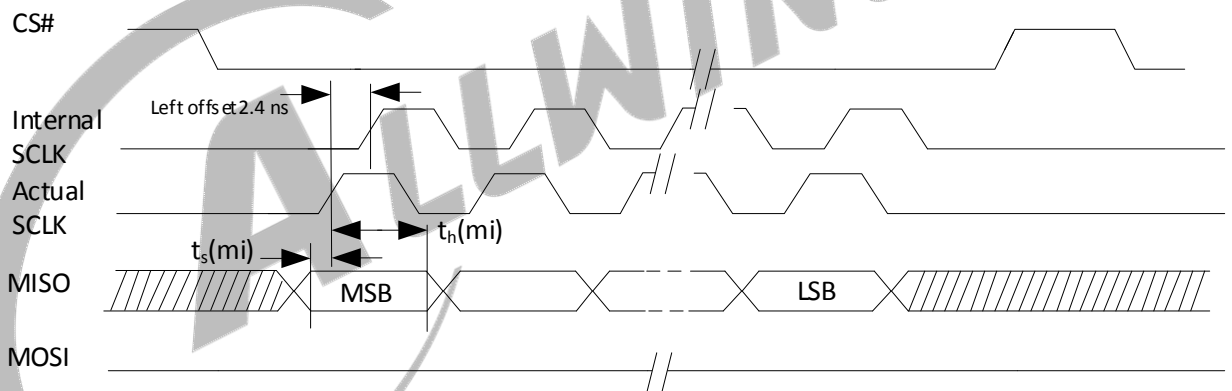


Table 5-25 SPI Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------|-----------|-----|---------------|-----|------|
| CS# active setup time | $t_s(cs)$ | - | $2T^{(1)}$ | - | ns |
| CS# active hold time | $t_h(cs)$ | - | $2T^{(1)}$ | - | ns |
| Data output delay time | $t_d(mo)$ | - | $T^{(1)}/2-3$ | - | ns |
| Data output hold time | $t_h(mo)$ | - | $T^{(1)}/2-3$ | - | ns |
| Data input setup time | $t_s(mi)$ | 0.2 | - | - | ns |
| Data input hold time | $t_h(mi)$ | 0.2 | - | - | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|--------|-----|-----|-----|------|
| (1).T is the cycle of clock. | | | | | |

5.12.5 SPI_DBI AC Electrical Characteristics

Figure 5-17 DBI 3-line Serial Interface Timing

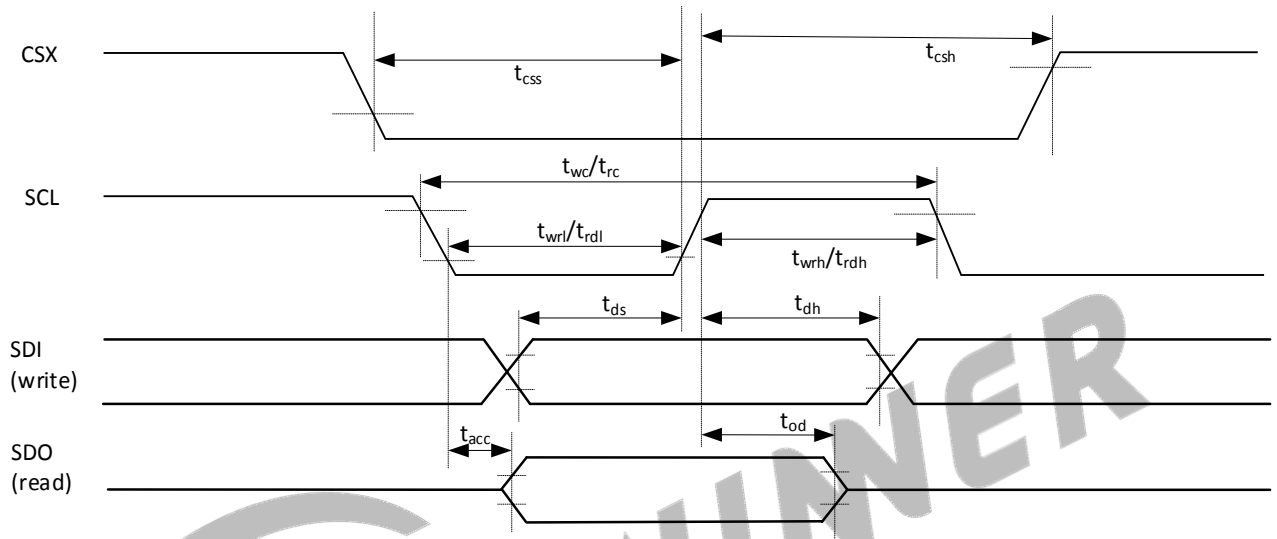


Table 5-26 DBI 3-line Serial Interface Timing Parameters

| Signal | Parameter | Symbol | Min | Max | Unit |
|--------------------|--------------------------------|------------|-----|-----|------|
| CSX | Chip select setup time (Write) | t_{css} | 15 | | ns |
| | Chip select setup time (Read) | t_{csh} | 60 | | ns |
| SCL (write) | Write cycle | t_{wc} | 16 | | ns |
| | Control pulse "H" duration | t_{wrh} | 7 | | ns |
| | Control pulse "L" duration | t_{wrl} | 7 | | ns |
| SCL (read) | Read cycle | t_{rc} | 150 | | ns |
| | Control pulse "H" duration | t_{rdh} | 60 | | ns |
| | Control pulse "L" duration | t_{rdl} | 60 | | ns |
| SDI/SDO (write) | Data setup time | t_{ds} | 7 | | ns |
| | Data hold time | t_{dt} | 7 | | ns |
| SDI/SDO | Read access time | t_{racc} | 10 | 50 | ns |

| Signal | Parameter | Symbol | Min | Max | Unit |
|--------|---------------------|----------|-----|-----|------|
| (read) | Output disable time | t_{od} | 15 | 50 | ns |

Figure 5-18 DBI 4-line Serial Interface Timing

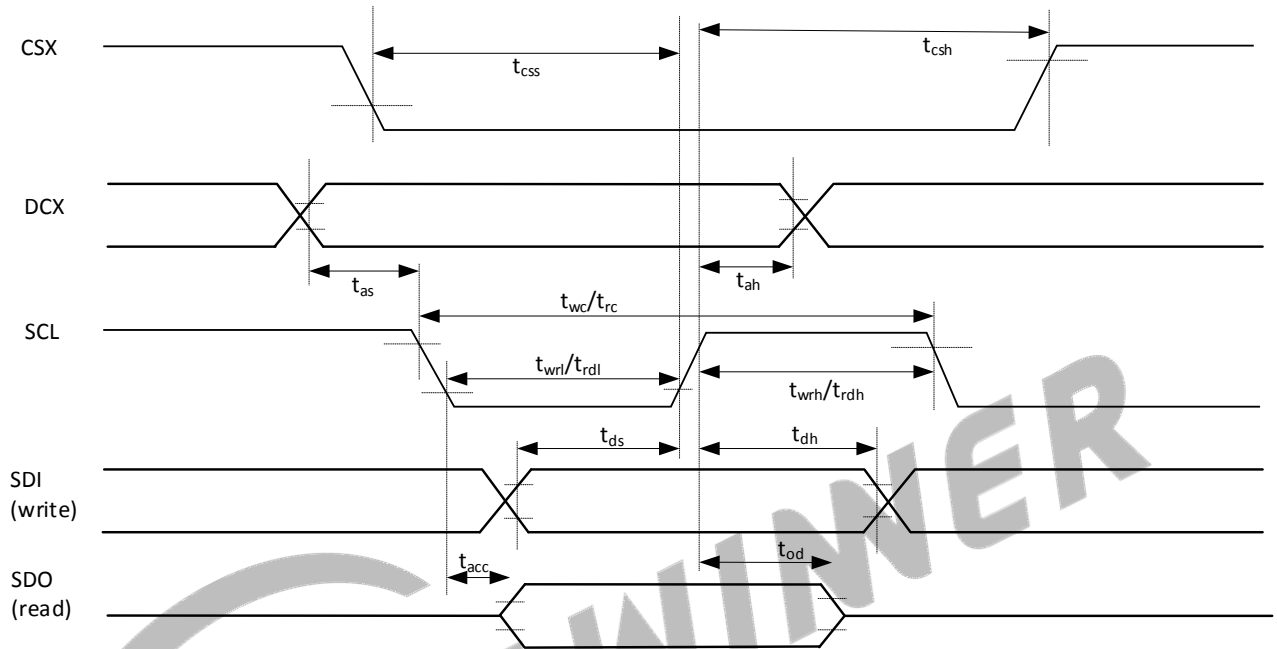


Table 5-27 DBI 4-line Serial Interface Timing Parameters

| Signal | Parameter | Symbol | Min | Max | Unit |
|----------------|--------------------------------|-----------|-----|-----|------|
| CSX | Chip select setup time (Write) | t_{css} | 15 | | ns |
| | Chip select setup time (Read) | t_{csh} | 60 | | ns |
| DCX | Address setup time | t_{as} | 10 | | ns |
| | Address hold time (Write/Read) | t_{ah} | 10 | | ns |
| SCL (write) | Write cycle | t_{wc} | 16 | | ns |
| | Control pulse "H" duration | t_{wrh} | 7 | | ns |
| | Control pulse "L" duration | t_{wrl} | 7 | | ns |
| SCL (read) | Read cycle | t_{rc} | 150 | | ns |
| | Control pulse "H" duration | t_{rdh} | 60 | | ns |
| | Control pulse "L" duration | t_{rdl} | 60 | | ns |

| Signal | Parameter | Symbol | Min | Max | Unit |
|--------------------|---------------------|------------|-----|-----|------|
| SDI/SDO (write) | Data setup time | t_{ds} | 7 | | ns |
| | Data hold time | t_{dt} | 7 | | ns |
| SDI/SDO (read) | Read access time | t_{racc} | - | 50 | ns |
| | Output disable time | t_{od} | 15 | 50 | ns |

5.12.6 UART AC Electrical Characteristics

Figure 5-19 UART RX Timing

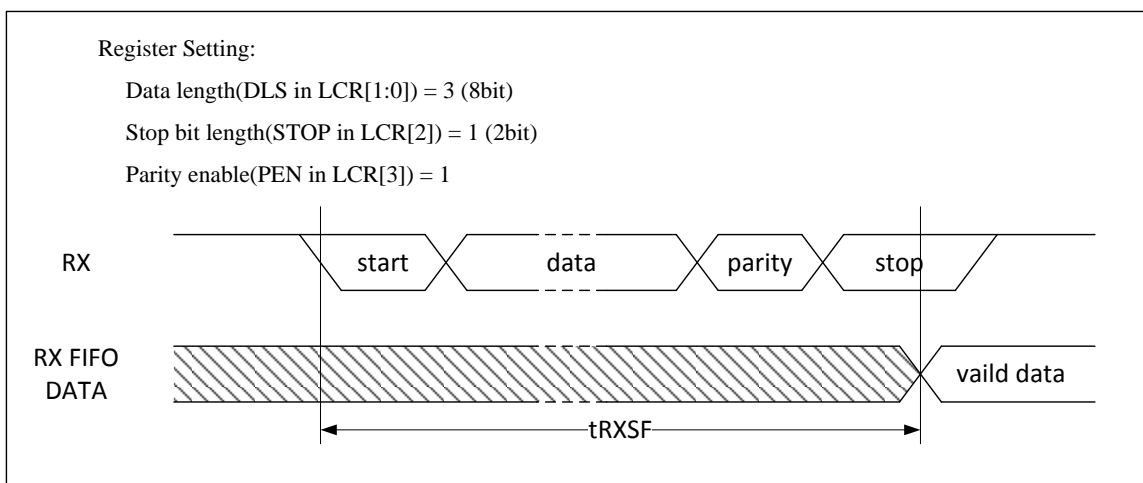


Figure 5-20 UART nCTS Timing

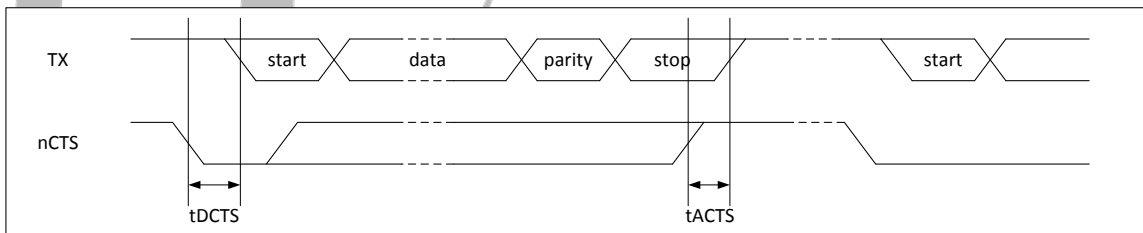


Figure 5-21 UART nRTS Timing

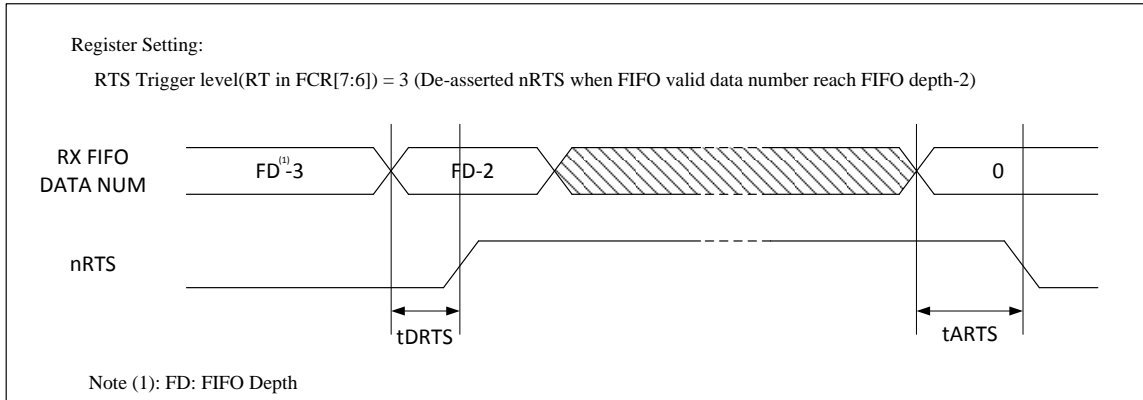


Table 5-28 UART Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------|---------------------------|-----|-------------------------|------|
| RX start to RX FIFO | tRXSF | 10.5 * BRP ⁽¹⁾ | - | 11 * BRP ⁽¹⁾ | ns |
| Delay time of de-asserted nCTS to TX start | tDCTS | - | - | BRP ⁽¹⁾ | ns |
| Step time of asserted nCTS to stop next transmission | tACTS | BRP ⁽¹⁾ /4 | - | - | ns |
| Delay time of de-asserted nRTS | tDRTS | - | - | BRP ⁽¹⁾ | ns |
| Delay time of asserted nRTS | tARTS | - | - | BRP ⁽¹⁾ | ns |

(1). BRP: Baud-Rate Period.

5.12.7 TWI AC Electrical Characteristics

Figure 5-22 TWI Timing

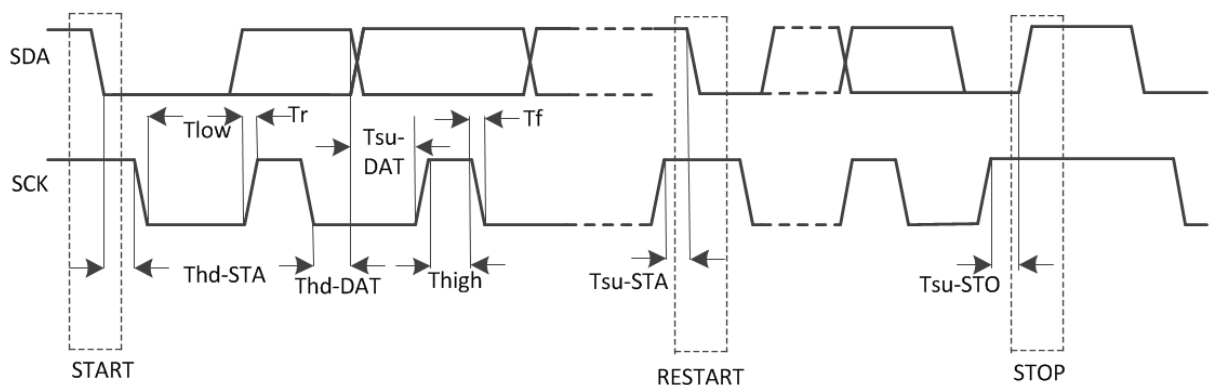


Table 5-29 TWI Timing Parameters

| Parameter | Symbol | Standard mode | | Fast mode | | Unit |
|----------------------|---------|---------------|------|-----------|-----|------|
| | | Min | Max | Min | Max | |
| SCK clock frequency | Fsck | 0 | 100 | 0 | 400 | kHz |
| Setup time in Start | Tsu-STA | 4.7 | - | 0.6 | - | us |
| Hold time in Start | Thd-STA | 4.0 | - | 0.6 | - | us |
| Setup time in Data | Tsu-DAT | 250 | - | 100 | - | ns |
| Hold time in Data | Thd-DAT | 5.0 | - | - | - | ns |
| Setup time in Stop | Tsu-STO | 4.0 | - | 6.0 | - | us |
| SCK low level time | Tlow | 4.7 | - | 1.3 | - | us |
| SCK high level time | Thigh | 4.0 | - | 0.6 | - | ns |
| SCK/SDA falling time | Tf | - | 300 | 20 | 300 | ns |
| SCK/SDA rising time | Tr | - | 1000 | 20 | 300 | ns |

5.12.8 I2S/PCM AC Electrical Characteristics

Figure 5-23 I2S/PCM Timing in Master Mode

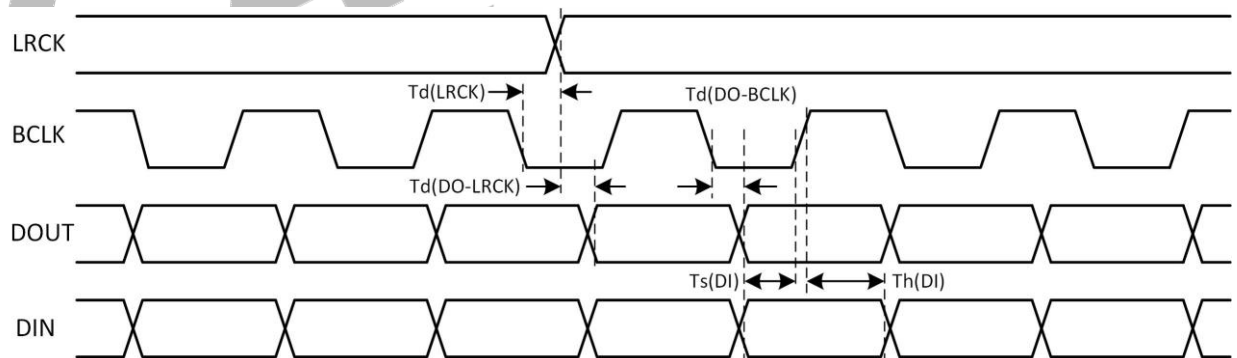


Table 5-30 I2S/PCM Timing Constants in Master Mode

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|--------------------------|-----|-----|-----|------|
| LRCK delay | T _d (LRCK) | - | - | 10 | ns |
| LRCK to DOUT delay (For LIF) | T _d (DO-LRCK) | - | - | 10 | ns |
| BCLK to DOUT delay | T _d (DO-BCLK) | - | - | 10 | ns |

| | | | | | |
|----------------|-----------|---|---|---|----|
| DIN setup | $T_s(DI)$ | 4 | - | - | ns |
| DIN hold | $T_h(DI)$ | 4 | - | - | ns |
| BCLK rise time | T_r | - | - | 8 | ns |
| BCLK fall time | T_f | - | - | 8 | ns |

Figure 5-24 I2S/PCM Timing in Slave Mode

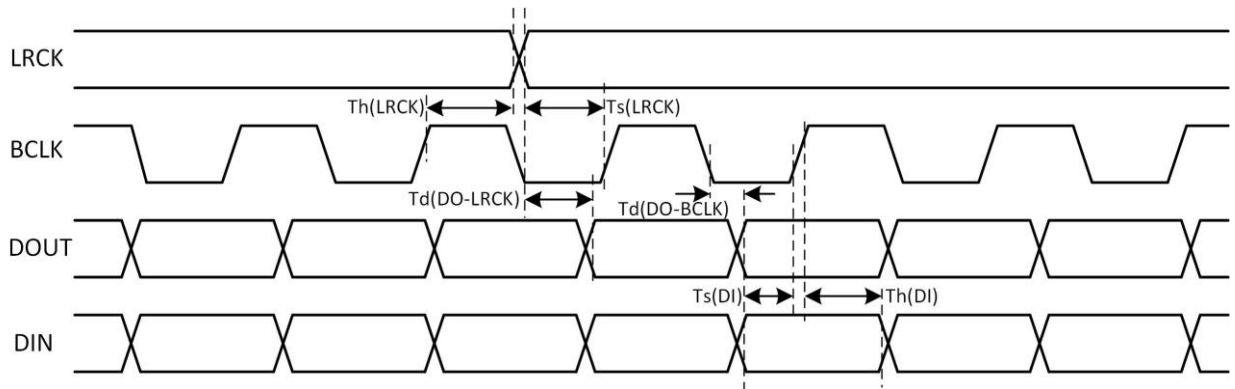


Table 5-31 I2S/PCM Timing Constants in Slave Mode

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|----------------|-----|-----|-----|------|
| LRCK setup | $T_s(LRCK)$ | 4 | - | - | ns |
| LRCK hold | $T_h(LRCK)$ | 4 | - | - | ns |
| LRCK to DOUT delay (For LIF) | $T_d(DO-LRCK)$ | - | - | 10 | ns |
| BCLK to DOUT delay | $T_d(DO-BCLK)$ | - | - | 10 | ns |
| DIN setup | $T_s(DI)$ | 4 | - | - | ns |
| DIN hold | $T_h(DI)$ | 4 | - | - | ns |
| BCLK rise time | T_r | - | - | 4 | ns |
| BCLK fall time | T_f | - | - | 4 | ns |

5.12.9 DMIC AC Electrical Characteristics

Figure 5-25 DMIC Timing

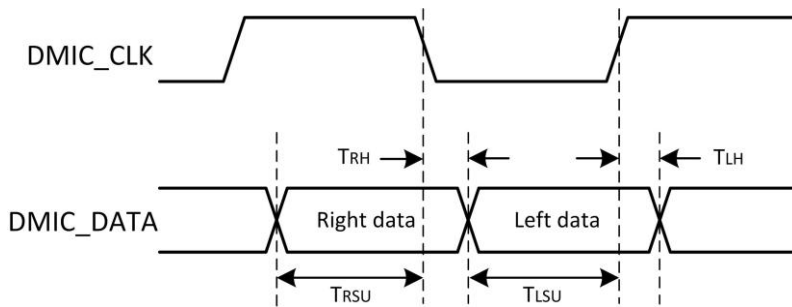


Table 5-32 DMIC Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|-----|-----|------|
| DMIC_DATA (Right) setup time to falling edge of DMIC_CLK | TRSU | 15 | - | - | ns |
| DMIC_DATA (Right) hold time from falling edge of DMIC_CLK | TRH | 0 | - | - | ns |
| DMIC_DATA (Left) setup time to rising edge of DMIC_CLK | TLSU | 15 | - | - | ns |
| DMIC_DATA (Left) hold time from rising edge of DMIC_CLK | TLH | 0 | - | - | ns |

5.12.10 OWA AC Electrical Characteristics

Figure 5-26 OWA Timing

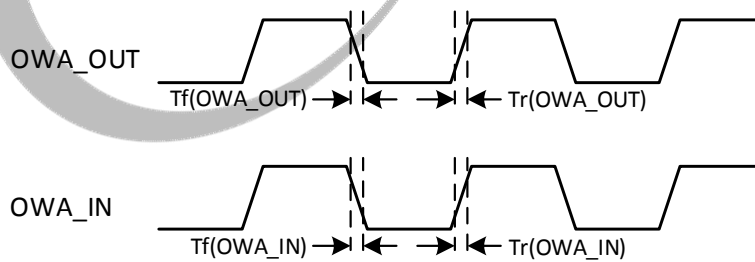


Table 5-33 OWA Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|-------------------|-------------|-----|-----|-----|------|
| OWA_OUT rise time | Tr(OWA_OUT) | - | - | 8 | ns |
| OWA_OUT fall time | Tf(OWA_OUT) | - | - | 8 | ns |
| OWA_IN rise time | Tr(OWA_IN) | - | - | 4 | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------|------------|-----|-----|-----|------|
| OWA_IN fall time | Tf(OWA_IN) | - | - | 4 | ns |

5.12.11 CIR_RX AC Electrical Characteristics

Figure 5-27 CIR_RX Timing

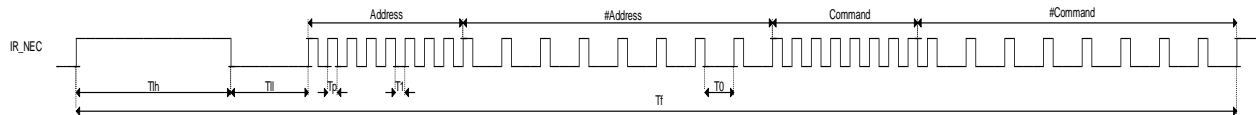


Table 5-34 CIR_RX Timing Constants

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------|--------|-----|------|-----|------|
| Frame period | Tf | - | 67.5 | - | ms |
| Lead code high time | Tlh | - | 9 | - | ms |
| Lead code low time | Tll | - | 4.5 | - | ms |
| Pulse time | Tp | - | 560 | - | us |
| Logical 1 low time | T1 | - | 1680 | - | us |
| Logical 0 low time | T0 | - | 560 | - | us |

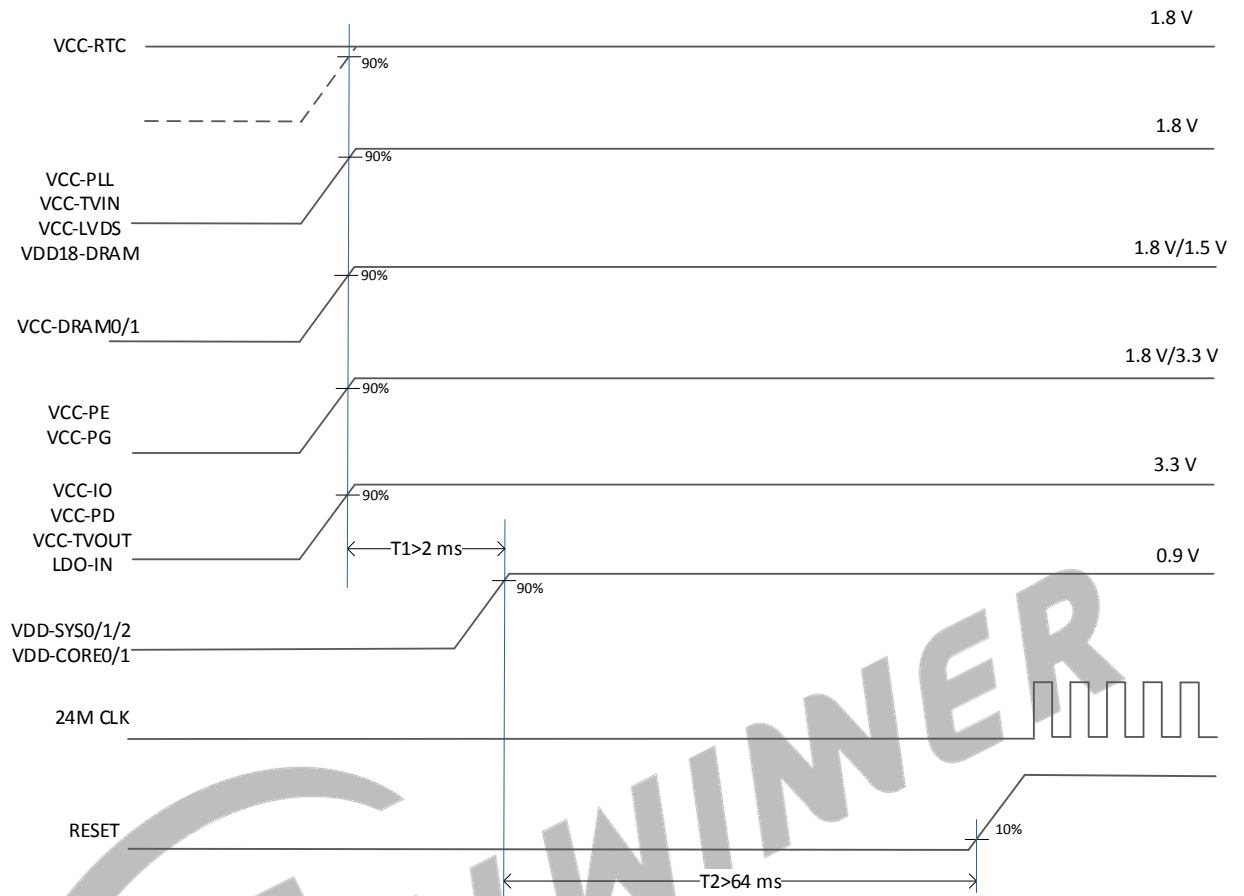
5.13 Power-On and Power-Off Sequence

5.13.1 Power-On Sequence

Figure 5-28 shows an example of the power-on sequence for the F133 device. The description of the power-on sequence is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90–110% of their nominal voltage, unless stated otherwise.
- VCC-RTC must be ramped no later than other power rails.
- VCC-IO must be ramped before VDD-SYS and VDD-CORE with a minimum delay of 2 ms.
- VCC-DRAM needs be stable before SDRAM driver initialization.
- During the entire power on sequence, the RESET signal must be held on low until all other power rails (except 24 MHz CLK) are stable for more than 64 ms.
- 24MHz clock starts oscillating after the RESET signal is released.

Figure 5-28 Power-On Timing

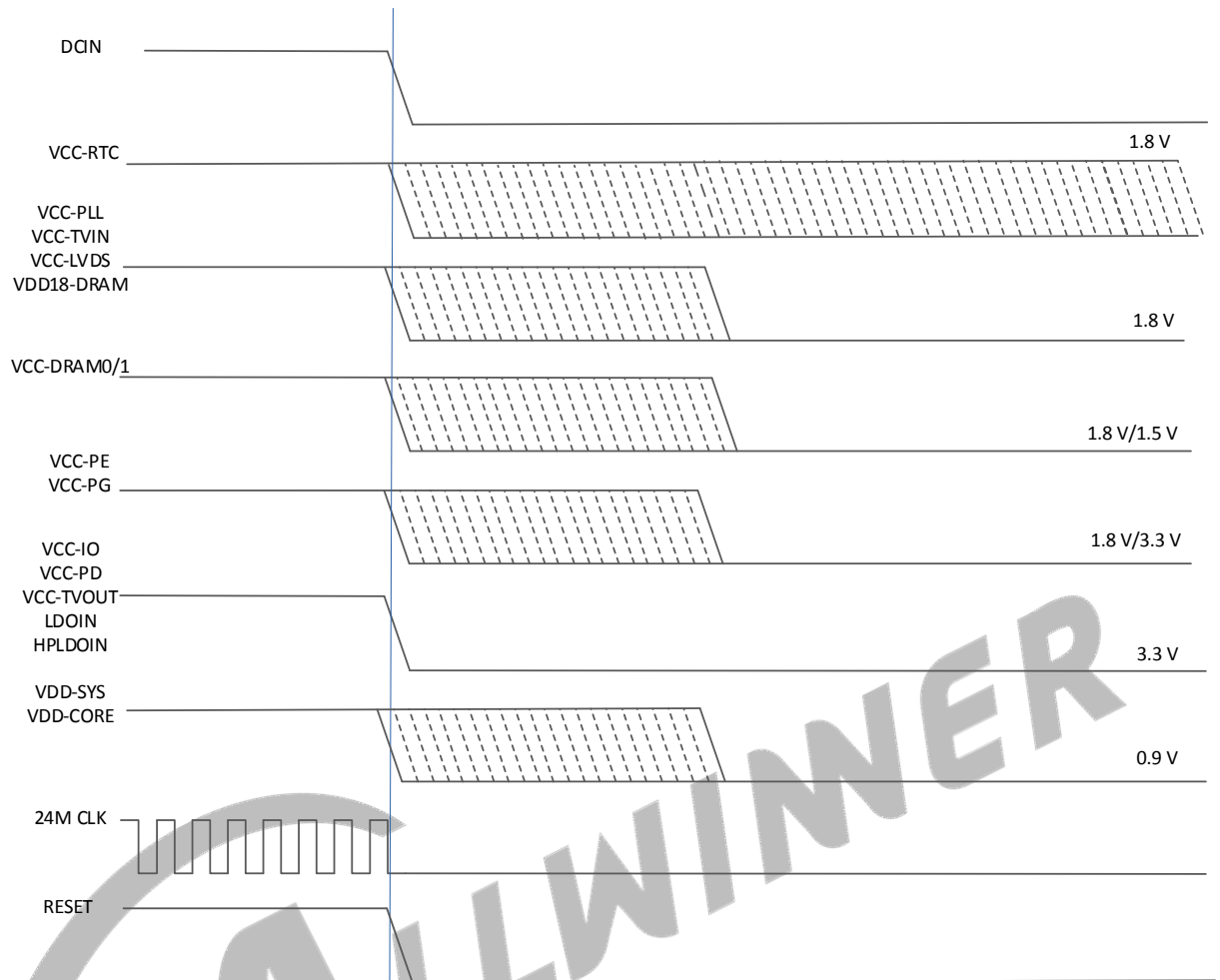


5.13.2 Power-Off Sequence

The power-off requirements are as follows.

- After the RESET signal goes low, the 24 MHz clock starts to stop oscillating.
- No special restrictions for other power rails.

Figure 5-29 Power-Off Timing



6 Package Thermal Characteristics

The maximum chip junction temperature ($T_J \text{ max}$) must never exceed the values given in [Table 5-2 Recommended Operating Conditions](#).

The maximum chip-junction temperature $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_a \text{ max} + (P_D \text{ max} \times \theta_{JA})$$

Where:

$T_a \text{ max}$ is the maximum ambient temperature in °C.

$P_D \text{ max}$ is the maximum power dissipation.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

°C/W = degrees Celsius per watt.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the F133. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-1 F133 Package Thermal Characteristics

| Symbol | Parameter | Min | Typ ⁽¹⁾ | Max | Unit |
|---------------|--|-----|--------------------|-----|------|
| θ_{JA} | Junction-to-Ambient Thermal Resistance | - | 20.36 | - | °C/W |
| θ_{JB} | Junction-to-Board Thermal Resistance | - | 7.43 | - | °C/W |
| θ_{JC} | Junction-to-Case Thermal Resistance | - | 5.52 | - | °C/W |

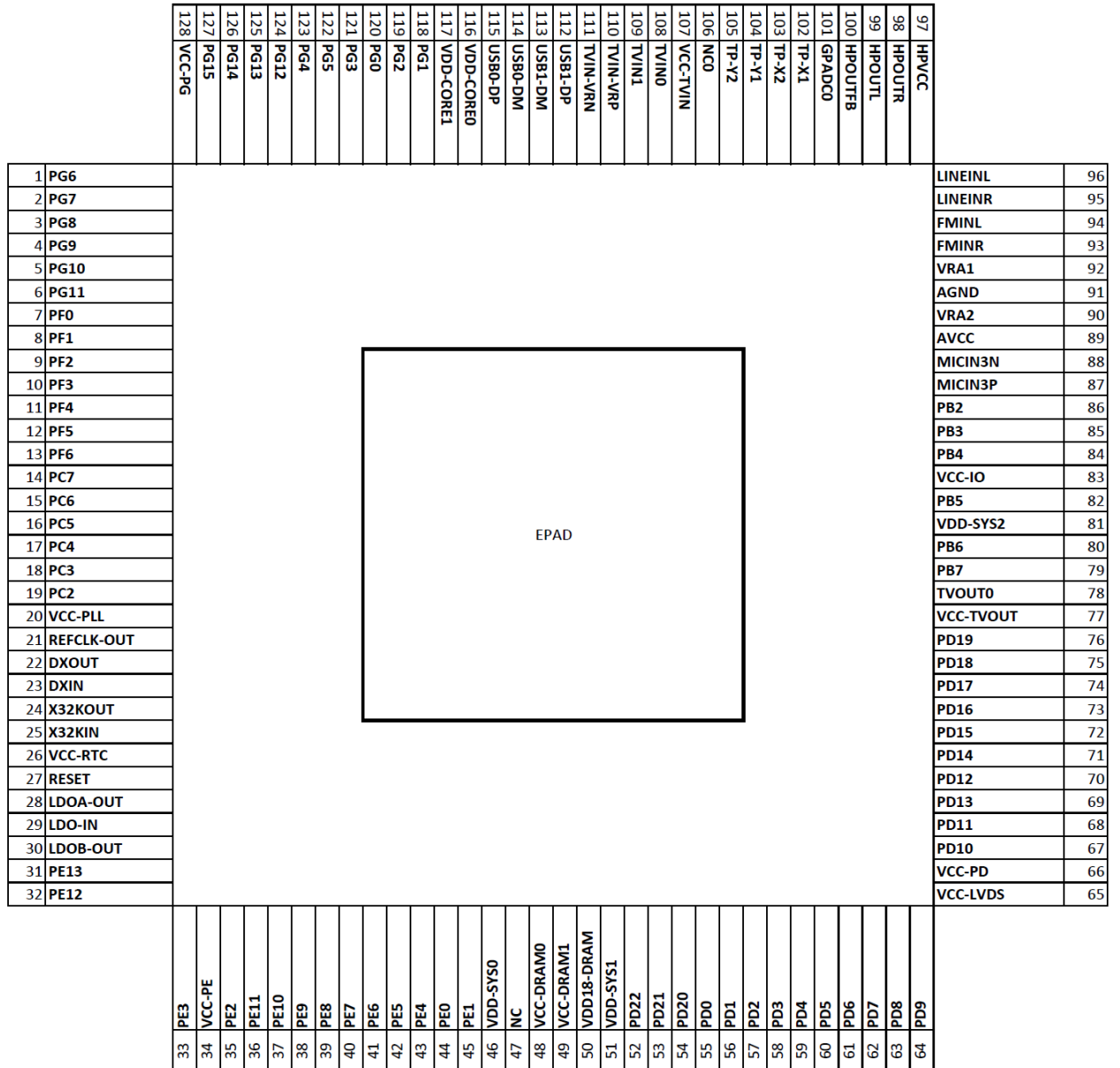
1. Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

7 Pin Assignment

7.1 Pin Map

For F133, eLQFP128, 14 mm x 14 mm package is offered. The following figure shows the pin map of the F133.

Figure 7-1 F133 Pin Map



The pin map difference between F133-A and F133-B is as follows.

Table 7-1 Pin Map Difference between F133-A and F133-B

| Pin No. | F133-A | F133-B |
|---------|--------|----------|
| 107 | NC | VCC-TVIN |
| 108 | NC | TVIN0 |

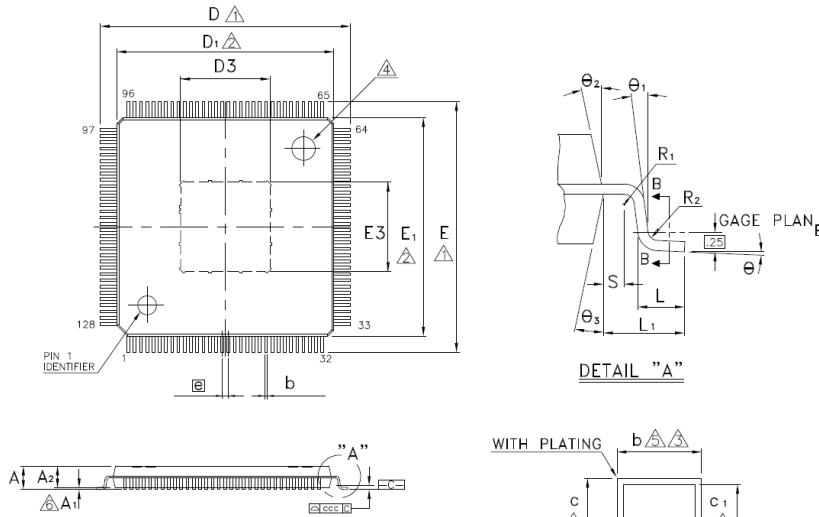
| Pin No. | F133-A | F133-B |
|---------|--------|----------|
| 109 | NC | TVIN1 |
| 110 | NC | TVIN-VRP |
| 111 | NC | TVIN-VRN |

 ALLWINNER

7.2 Package Dimension

Figure 7-2 shows the top, bottom, and side views of F133 package dimension.

Figure 7-2 F133 Package Dimension



NOTE :

- ▲ TO BE DETERMINED AT SEATING PLANE E_{CC} .
- ▲ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- ▲ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ▲ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- ▲ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
- ▲ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 7. CONTROLLING DIMENSION : MILLIMETER.
- 8. REFERENCE DOCUMENT : JEDEC MS-026.
- 9. SPECIAL CHARACTERISTICS C CLASS: ccc

| Symbol | Dimension in mm | | | Dimension in inch | | |
|----------------|-----------------|-------|-------|-------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| A ₁ | 0.025 | — | 0.127 | 0.001 | — | 0.005 |
| A ₂ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| b ₁ | 0.13 | 0.16 | 0.19 | 0.005 | 0.006 | 0.007 |
| c | 0.09 | 0.14 | 0.20 | 0.004 | 0.006 | 0.008 |
| c ₁ | 0.09 | 0.12 | 0.16 | 0.004 | 0.005 | 0.006 |
| D | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| D ₁ | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| E ₁ | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| ⓐ | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L ₁ | 1.00 REF | | | 0.039 REF | | |
| R ₁ | 0.08 | — | — | 0.003 | — | — |
| R ₂ | 0.08 | — | — | 0.003 | — | — |
| S | 0.20 | — | — | 0.008 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ ₁ | 0° | — | — | 0° | — | — |
| θ ₂ | 11° | 12° | 13° | 11° | 12° | 13° |
| θ ₃ | 11° | 12° | 13° | 11° | 12° | 13° |
| ccc | 0.08 | | | 0.003 | | |

| L/F | Exposed Pad Size | |
|-----|-----------------------|-------------------|
| | Dimension in mm | Dimension in inch |
| ① | D3/E3 3.61 REF | 0.142 REF |
| ② | D3/E3 5.72 REF | 0.225 REF |
| ③ | D3/E3 8.00 REF | 0.315 REF |
| ④ | D3/E3 7.75 / 6.60 REF | 0.305 / 0.260 REF |
| ⑤ | D3/E3 5.60 / 5.20 REF | 0.221 / 0.205 REF |
| ⑥ | D3/E3 5.72 / 5.46 REF | 0.225 / 0.215 REF |



8 Carrier, Storage and Baking Information

8.1 Carrier

8.1.1 Matrix Tray Information

Table 8-1 shows the F133 matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

| Item | Color | Size | Note |
|---|---------------|--|--|
| Tray | Black | 315 mm x 136 mm x 7.62 mm | 90 Qty/Tray |
| Aluminum foil bags | Silvery white | 540 mm x 300 mm x 0.14 mm | Vacuum packing Including HIC and desiccant Printing: RoHS symbol |
| Pearl cotton cushion (Vacuum bag) | White | 12 mm x 680 mm x 185 mm | |
| Pearl cotton cushion (The Gap between vacuum bag and inner box) | White | Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm | |
| Inner Box | White | 396 mm x 196 mm x 96 mm | Printing: RoHS symbol 10 Tray/Inner box |
| Carton | White | 420 mm x 410 mm x 320 mm | 6 Inner box/Carton |

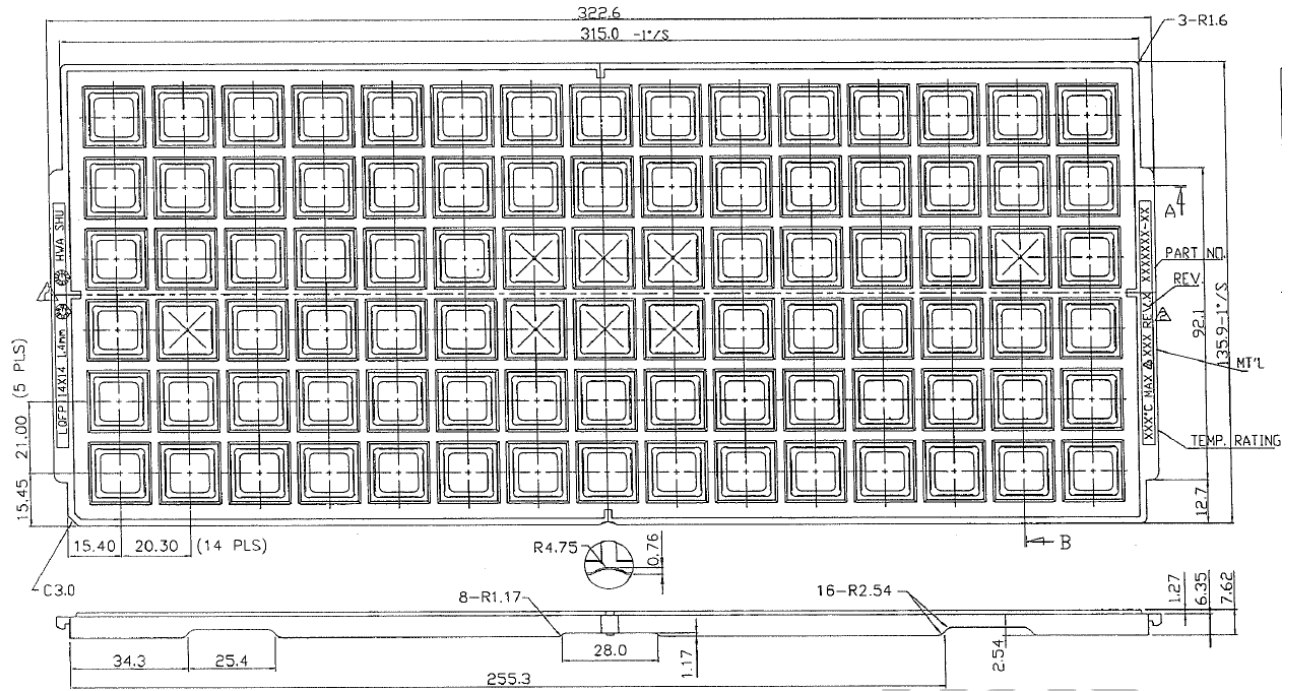
Table 8-2 shows the F133 packing quantity.

Table 8-2 F133 Packing Quantity Information

| Sample | Size (mm) | Qty/Tray | Tray/Inner Box | Full Inner Box Qty | Inner Box/Carton | Full Carton Qty |
|-------------------|-----------|----------|----------------|--------------------|------------------|-----------------|
| F133-A, F133-B | 14 x 14 | 90 | 10 | 900 | 6 | 5400 |

Figure 8-1 shows tray dimension drawing of the F133.

Figure 8-1 F133 Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.



NOTE

The F133 device samples are classified as MSL3.

Table 8-3 MSL Summary

| MSL | Out-of-bag floor life | Comments |
|-----|-----------------------|---------------|
| 1 | Unlimited | ≤30°C / 85%RH |
| 2 | 1 year | ≤30°C / 60%RH |
| 2a | 4 weeks | ≤30°C / 60%RH |
| 3 | 168 hours | ≤30°C / 60%RH |

| MSL | Out-of-bag floor life | Comments |
|-----|-----------------------|---------------|
| 4 | 72 hours | ≤30°C / 60%RH |
| 5 | 48 hours | ≤30°C / 60%RH |
| 5a | 24 hours | ≤30°C / 60%RH |
| 6 | Time on Label (TOL) | ≤30°C / 60%RH |

8.2.2 Bagged Storage Conditions

Table 8-4 defines the shelf life of the F133 device samples.

Table 8-4 Bagged Storage Conditions

| | |
|---------------------|----------------|
| Packing mode | Vacuum packing |
| Storage temperature | 20–26°C |
| Storage humidity | 40–60%RH |
| Shelf life | 12 months |

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of the F133 is as follows.

Table 8-5 Out-of-bag Duration

| | |
|--------------------------------|-----------|
| Storage temperature | 20–26°C |
| Storage humidity | 40–60%RH |
| Moisture sensitive level (MSL) | 3 |
| Floor life | 168 hours |

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake the F133 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the F133 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the F133 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.



9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

Figure 9-1 shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

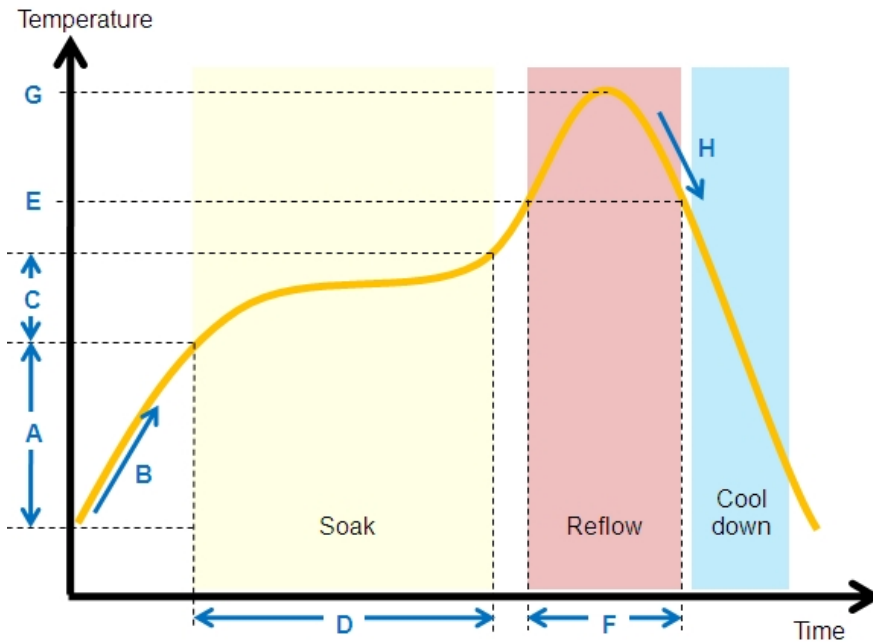


Table 9-1 Lead-free Reflow Profile Conditions

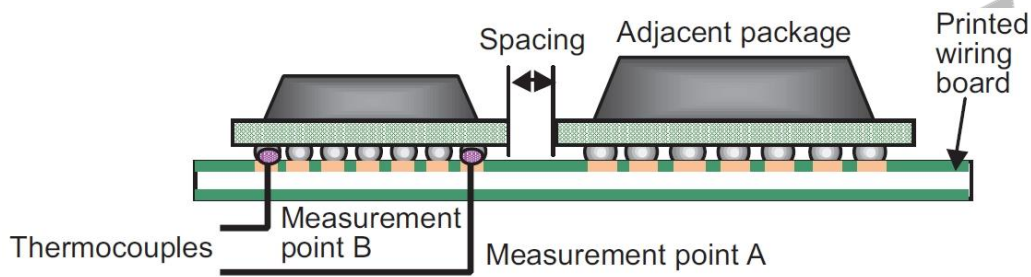
| | QTI typical SMT reflow profile conditions (for reference only) | |
|-------------|--|--------------------|
| | Step | Reflow condition |
| Environment | N2 purge reflow usage (yes/no) | Yes, N2 purge used |
| | If yes, O2 ppm level | O2 < 1500 ppm |
| A | Preheat ramp up temperature range | 25°C -> 150°C |
| B | Preheat ramp up rate | 1.5–2.5 °C/s |
| C | Soak temperature range | 150°C -> 190°C |
| D | Soak time | 80–110 s |
| E | Liquidus temperature | 217°C |
| F | Time above liquidus | 60–90 s |

| | QTI typical SMT reflow profile conditions (for reference only) | |
|---|--|------------------|
| | Step | Reflow condition |
| G | Peak temperature | 240–250°C |
| H | Cool down temperature rate | ≤4°C/s |

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 FT/QA/QC Test

10.1 FT Test

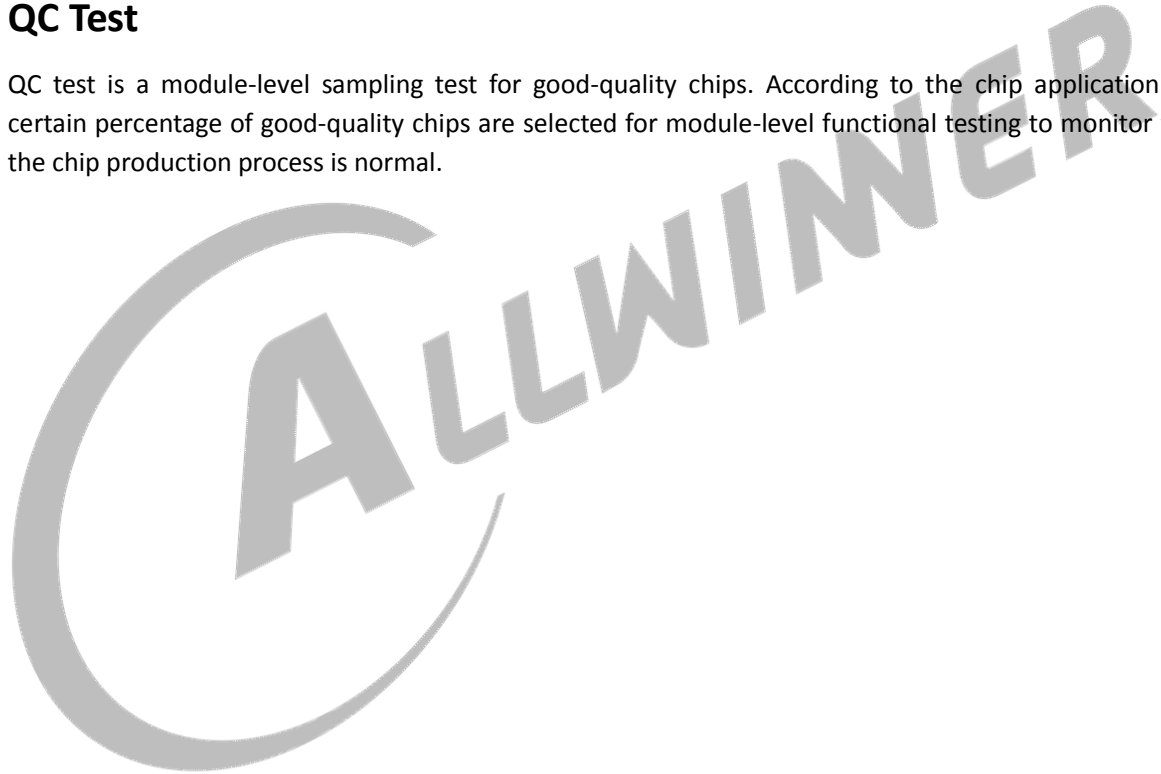
FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

10.2 QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

10.3 QC Test

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.



11 Part Marking

11.1 F133-A

Figure 11-1 shows the F133-A marking.

Figure 11-1 F133-A Marking

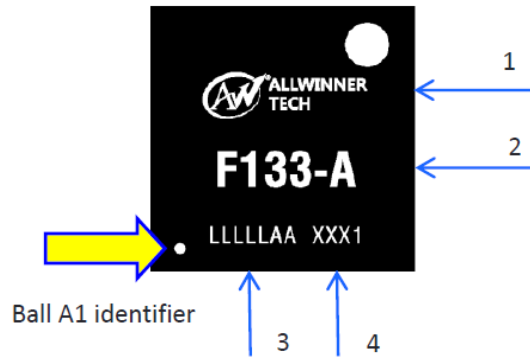


Table 11-1 describes the F133-A marking definitions.

Table 11-1 F133-A Marking Definitions

| No. | Marking | Description | Fixed/Dynamic |
|-----|---------------|------------------------|---------------|
| 1 | ALLWINNERTECH | Allwinner logo or name | Fixed |
| 2 | F133-A | Product name | Fixed |
| 3 | LLLLAA | Lot number | Dynamic |
| 4 | XXX1 | Date code | Dynamic |

11.2 F133-B

Figure 11-2 shows the F133-B marking.

Figure 11-2 F133-B Marking

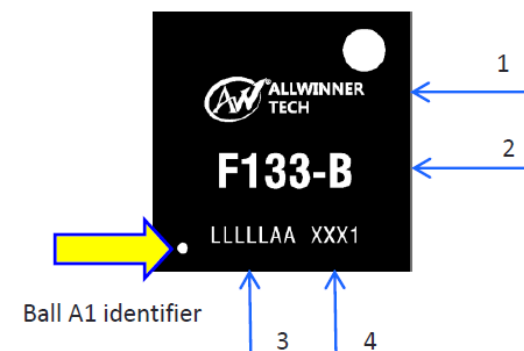


Table 11-2 describes the F133-B marking definitions.

Table 11-2 F133-B Marking Definitions

| No. | Marking | Description | Fixed/Dynamic |
|-----|---------------|------------------------|---------------|
| 1 | ALLWINNERTECH | Allwinner logo or name | Fixed |
| 2 | F133-B | Product name | Fixed |
| 3 | LLLLLAA | Lot number | Dynamic |
| 4 | XXX1 | Date code | Dynamic |



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